半导体之旅

--从量子理论到人工智能

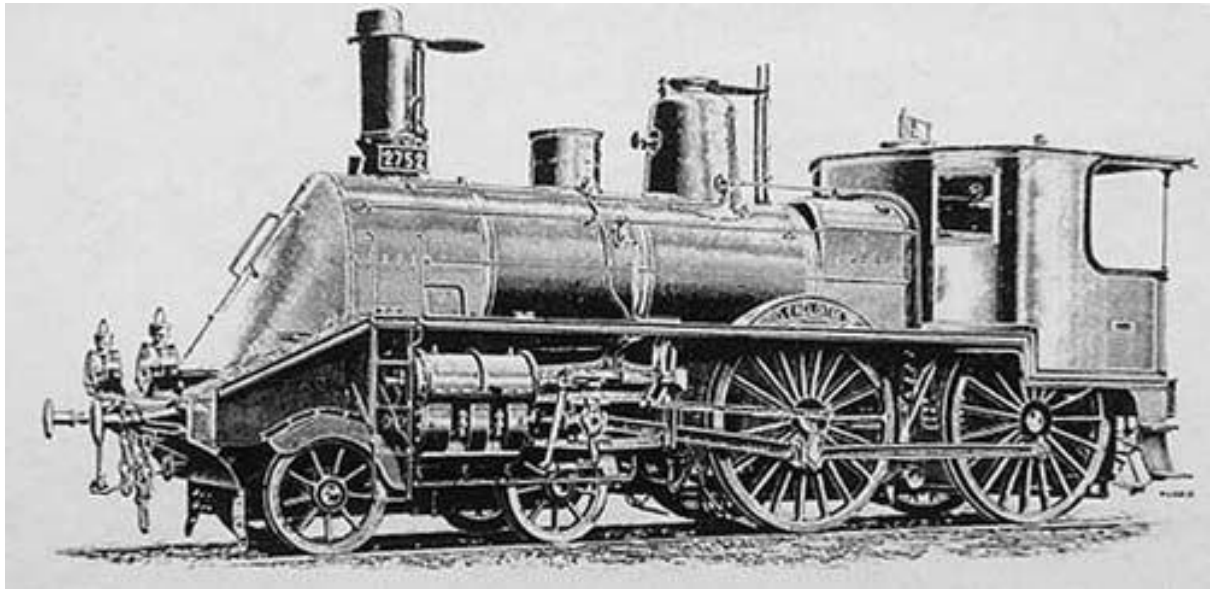
张俊

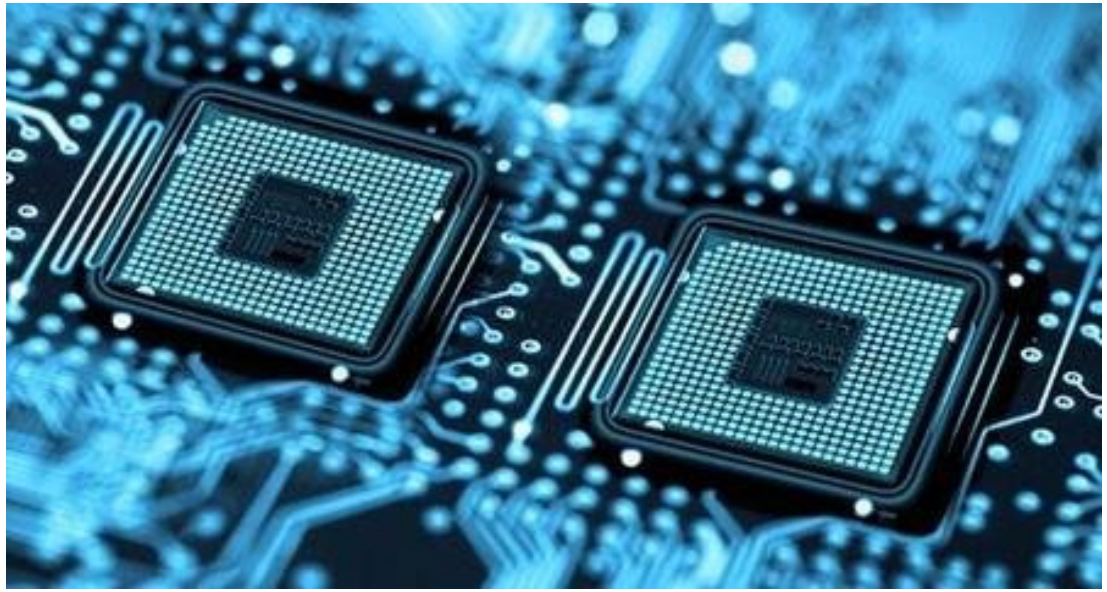
半导体芯片物理与器件全国重点实验室

中国科学院半导体研究所

zhangjwill@semi.ac.cn

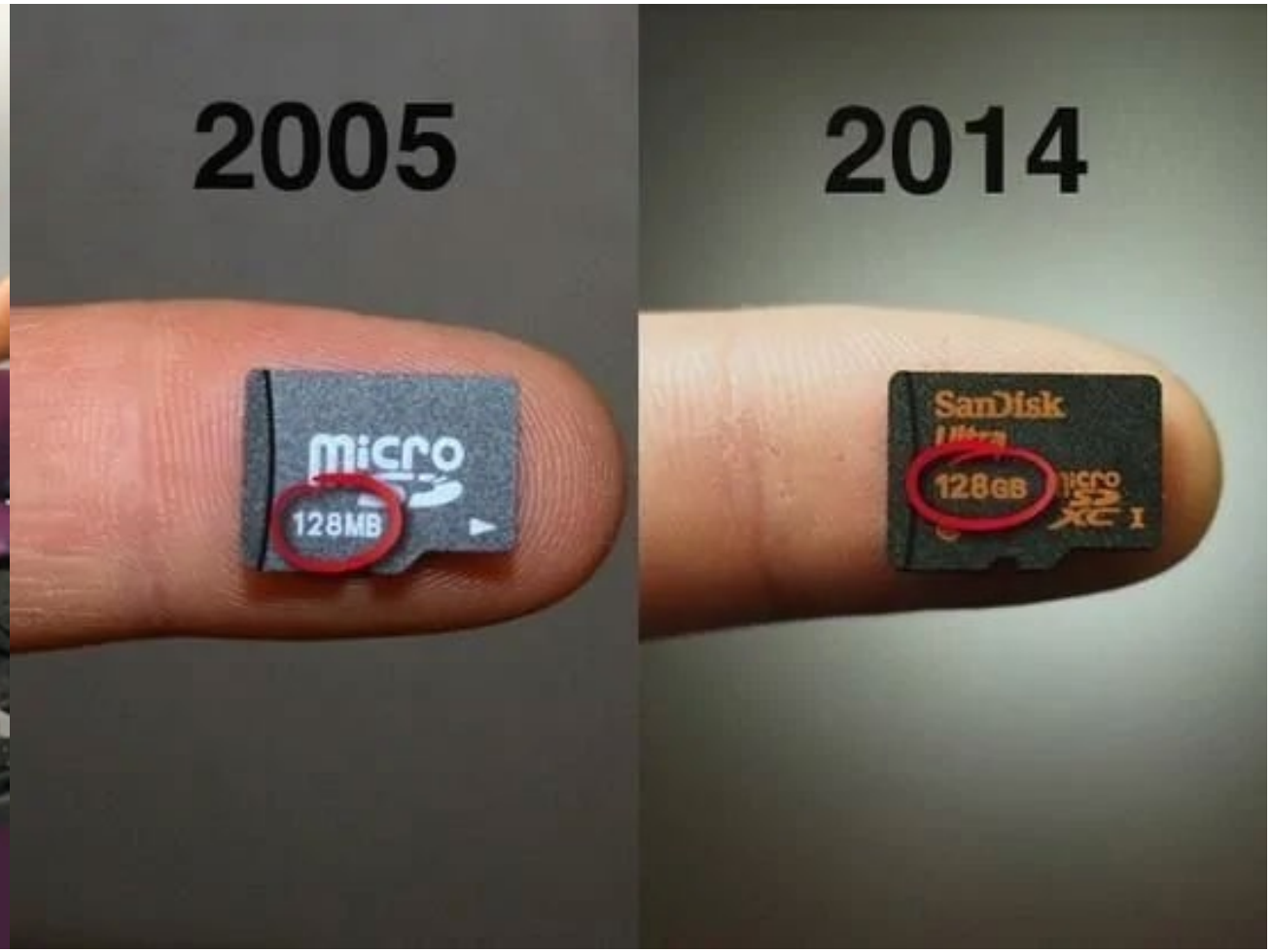
人类利用材料的发展过程





Amazing

1956
5MB


2005
micro
128MB
2014
SanDisk
128GB

SAMSUNG
V-NAND SSD
990 PRO
PCIe 4.0 NVMe M.2 SSD
4TB
www.samsung.com/ssd
SAMSUNG ELECTRONICS CO., LTD.

智能手机

智能手機功能多 1個打 50 個
1部手機=188克*
50樣東西=34公斤
*以iPhone 7 plus為例
Topick
hket.com

2005
Luca Bruno / AP

2013
NBC NEWS
Michael Sohn / AP

半导体物理是一切半导体技术的源头

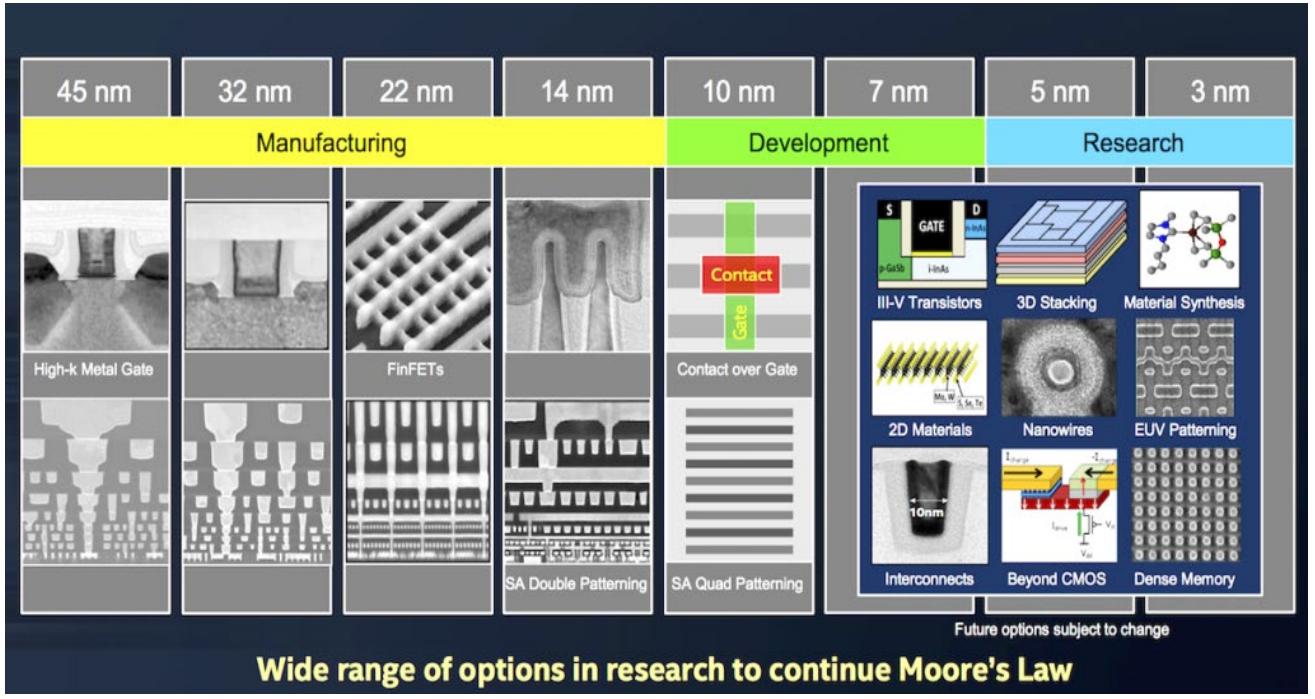
诺贝尔物理学奖：

- 1947年**晶体管**（1956）
- 1958年**集成电路**（2000）
- 1958年**隧道效应**（1973）
- 1960年**非晶半导体电子理论**（1977）
- 1963年**激光二极管**（2000）
- 1963年**快速晶体管**（2000）
- 1966年**光纤通信**（2009）
- 1969年**CCD图像传感器**（2009）
- 1980年**量子霍尔效应**（1985）
- 1982年**分数量子霍尔效应**（1998）
- 1993年**蓝光LED**（2014）

晶体管被誉为“20世纪最伟大的发明”

巴丁、肖克利、布拉顿

半导体是现代信息化社会的基石



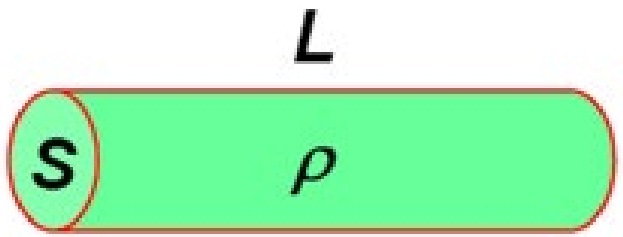
什么是半导体?

半导体：导电能力介于导体和绝缘体之间。

导体	半导体	绝缘体
10^{-6} —10^{-4}	10^{-4} —10^{10}	>10^{10}

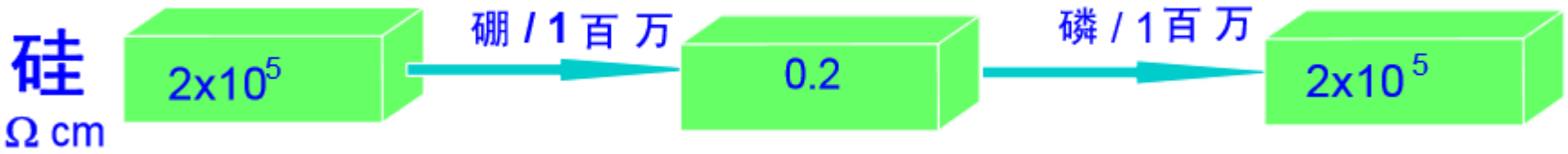
电阻率$\rho(\Omega.cm)$

$$R = \rho\frac{L}{S}$$



半导体的主要特点

（1）电阻率可以在很大范围内变化



硅的纯度仍然高达99.9999%

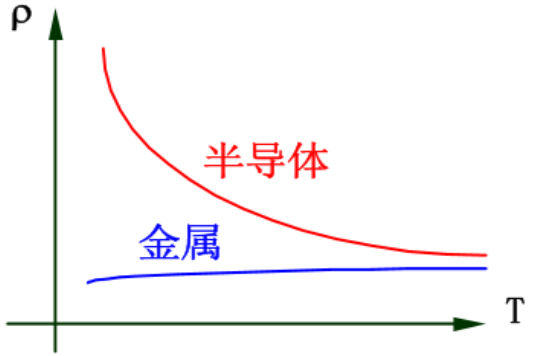
（2）温度对半导体的影响

T=300 K

$\rho = 2 \times 10^5 \Omega \cdot \mathrm{cm}$

T=320 K

$\rho = 2 \times 10^4 \Omega \cdot \mathrm{cm}$



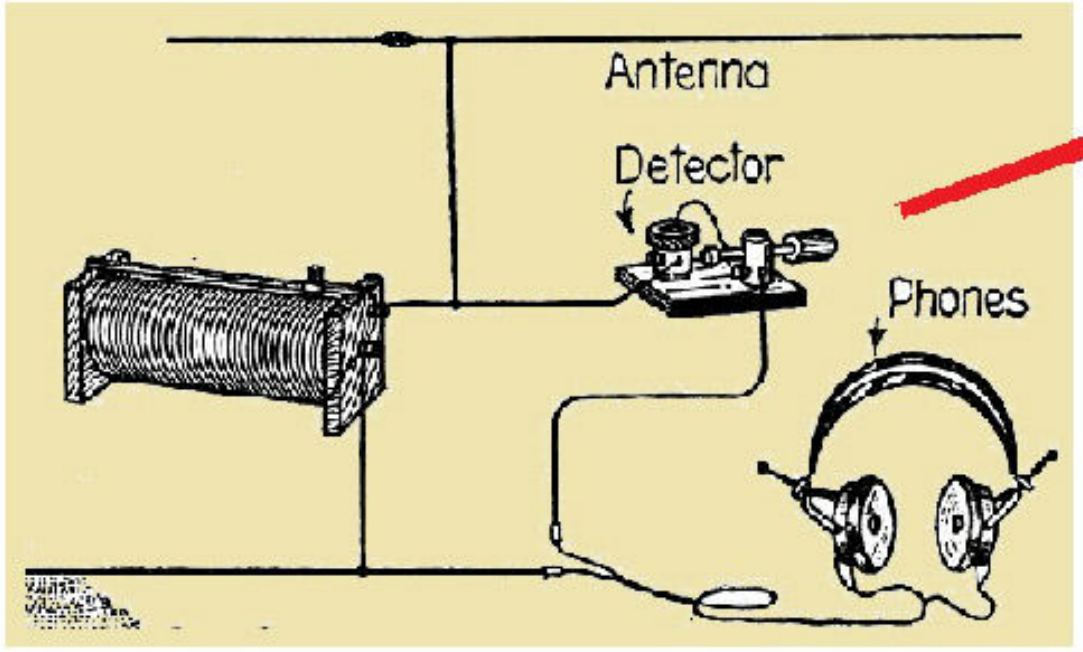
（3）光照对半导体的影响

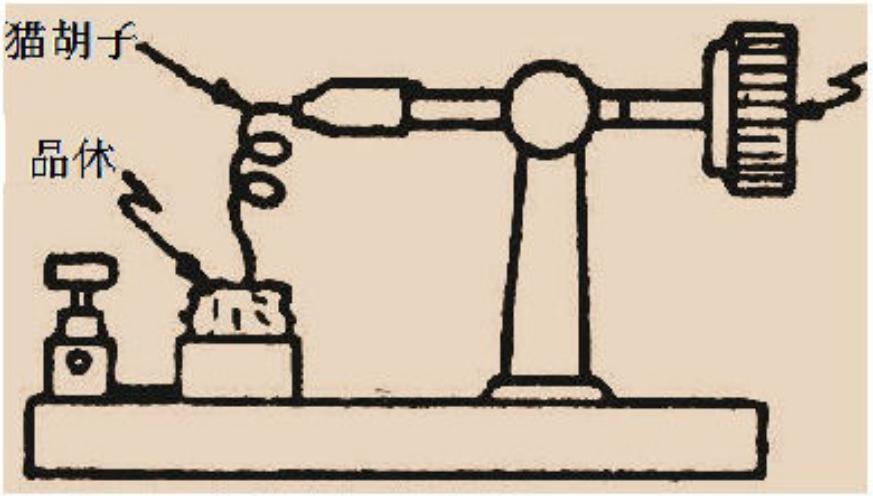
硫化镉(CdS)半导体薄膜，无光照时的暗电阻为几十MΩ， 当受光照后电阻值可以下降为几十KΩ

整流效应

- 1874年： F. Braun 首次发现半导体的整流效应

1883年：制造出硒整流器
1927年：制造出氧化亚铜整流器



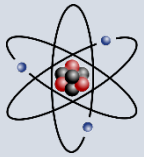


矿石收音机和猫胡子探测器

电子科学技术的发展

1897

The discovery of electron (1897)



Planetary Model (1909)

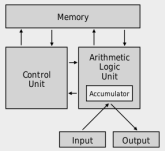
Bole Model (1913)

$$i\hbar \frac{\partial}{\partial t}\Psi(\boldsymbol{r},t) = \hat{H}\Psi(\boldsymbol{r},t)$$

Quantum mechanics (1925)

1940

Colossus computer(1925)



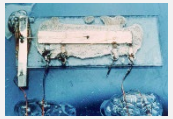
Von Neuman architecture (1945)

ENIAC (1946)

transistor (1947)

1950

Laser (1958)



IC (1958)

LED (1967)

1970

intel 4004 CPU (1971)

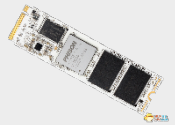
motorola cell phone (1973)

digital camera (1975)

Apple 2 (1977)

1980

IBM PC (1981)



Flash (1984)

Toshiba t1100 Notebook (1985)

WWW (1989)

1990

IBM Simon First Smart phone (1994)

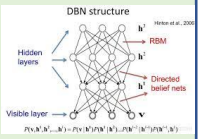
IBM Deep Blue(1997)

GPU NVIDIA GeForce 256 (1999)

3G (2000)

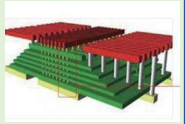
2000

Facebook (2004)



DBN (2006)

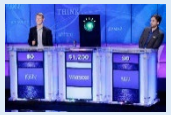
Apple1 Phone (2007)



Toshiba BICS 3D NAND (2007)

2010

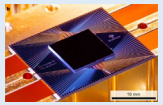
D-wave Quantum computer (2011)



Watson (2011)

4G (2014)

Alphago (2016))



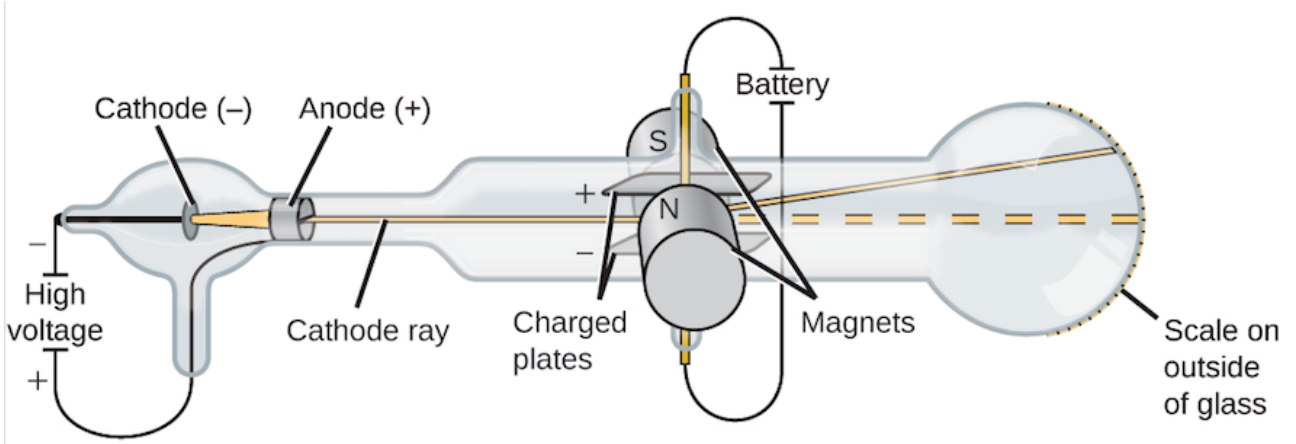
Google Quantum Computer (2019)

电子?

J. J. Thompson
(1856~1940)

J. J. 汤姆逊发现原子由称为电子的更小的带负电粒子组成。

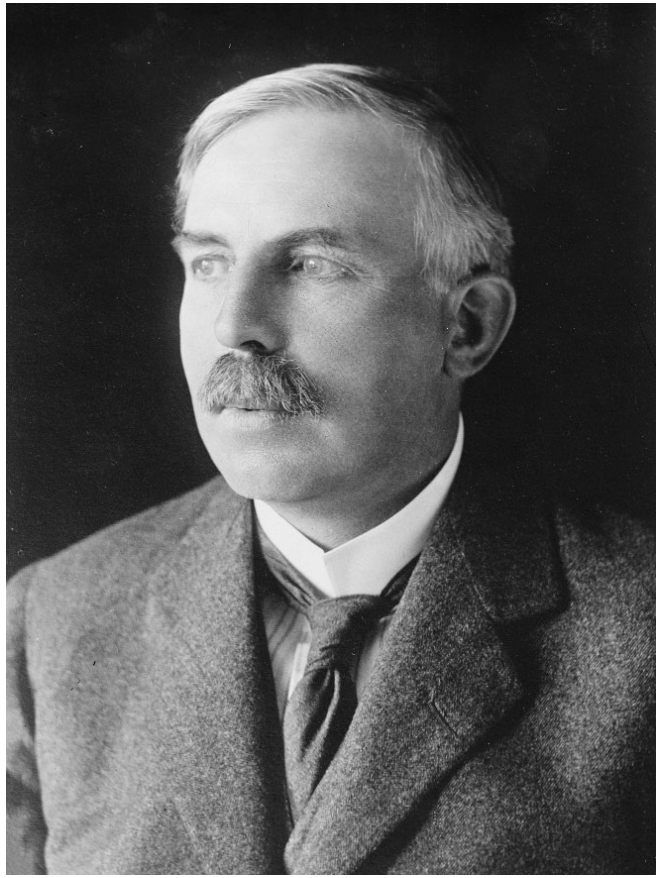
J. J. 汤姆逊的发现是通过进行“阴极射线管”实验的结果。



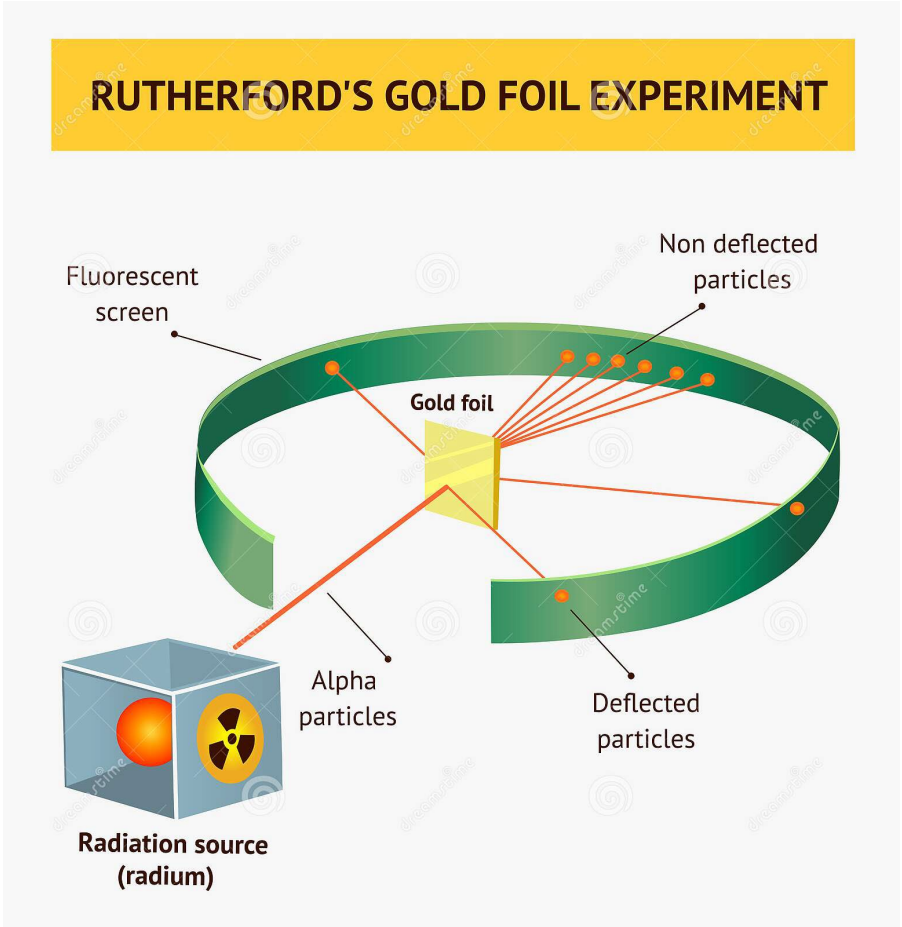
测量了电荷/质量比

卢瑟福散射

Rutherford Scattering



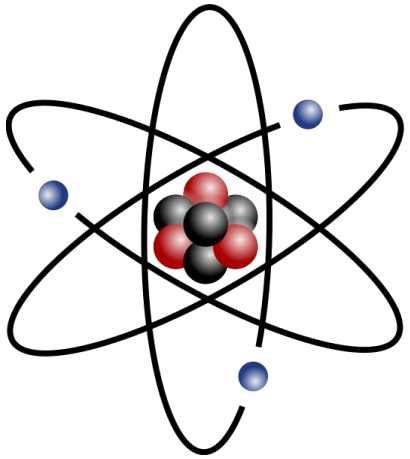
Ernest. Rutherford
(1871~1937)



原子结构

相对尺度

10^{-10} m



原子

10^{-14} m

原子核

原子

Raymond James Stadium

10^{-4}

原子核

99.97% of the mass

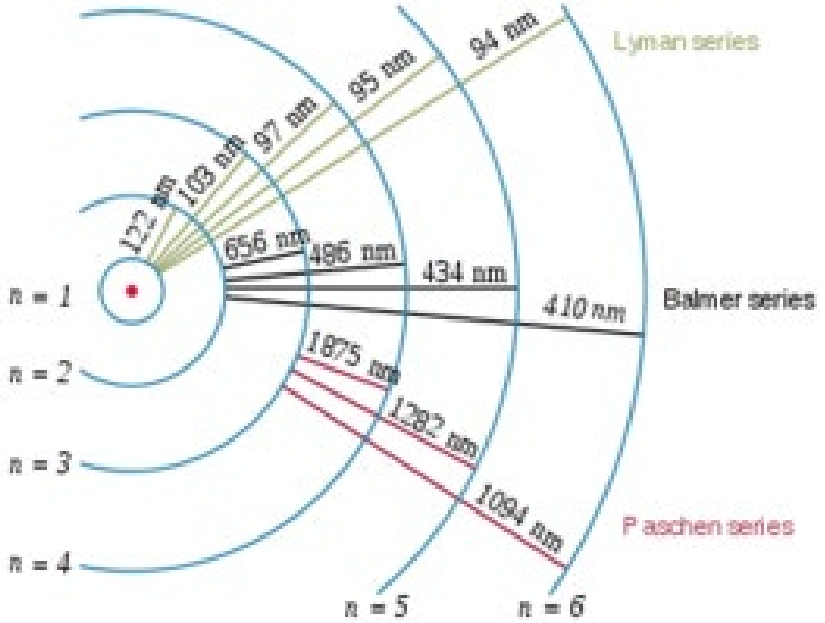
量子力学的确定性

尼尔斯·波尔

Niels Bohr(1885~1962)

1922年诺贝尔物理学奖得主，

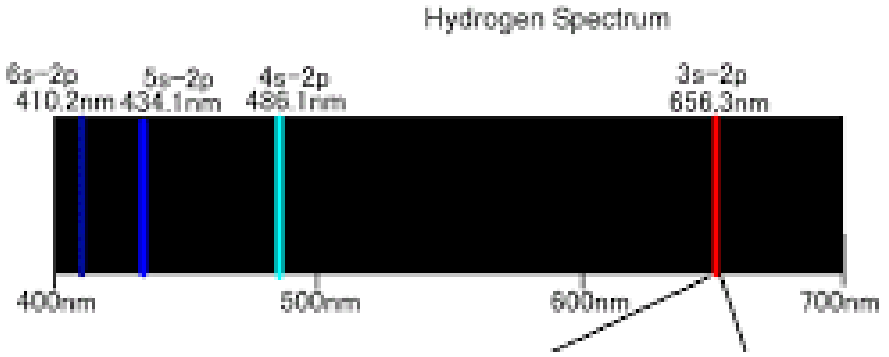
创建哥本哈根理论物理研究所



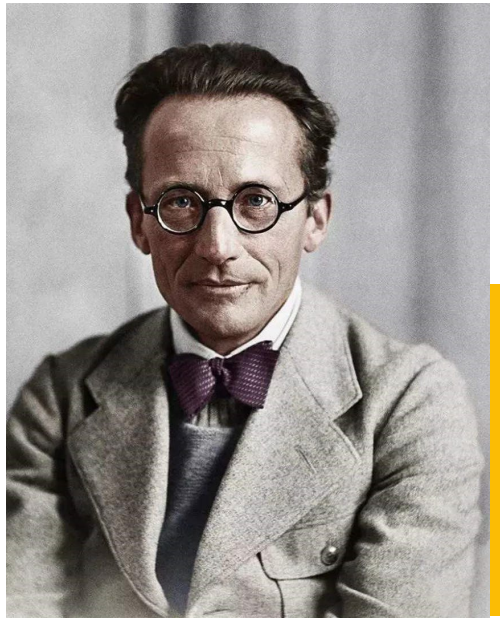
巴尔末系氢吸收光谱

$$\frac{1}{\lambda} = R_H(\frac{1}{2^2} - \frac{1}{n^2})$$

n=3, 4, 5，λ为吸收或发射谱线波长，R_H为常数



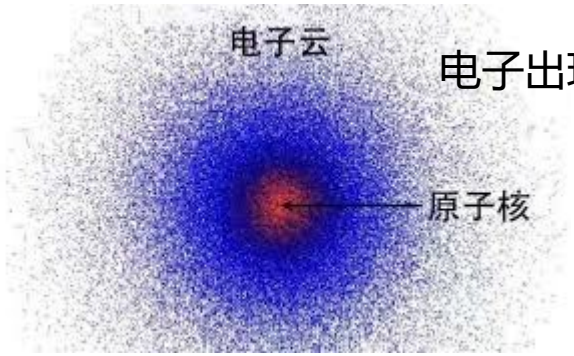
量子力学的不确定性，波粒二象性



奥地利物理学家：薛定谔

E. Schrödinger (1887~1961)

$$i\hbar\frac{\partial}{\partial t}\Psi(\mathbf{r},t)=\hat{H}\Psi(\mathbf{r},t)$$

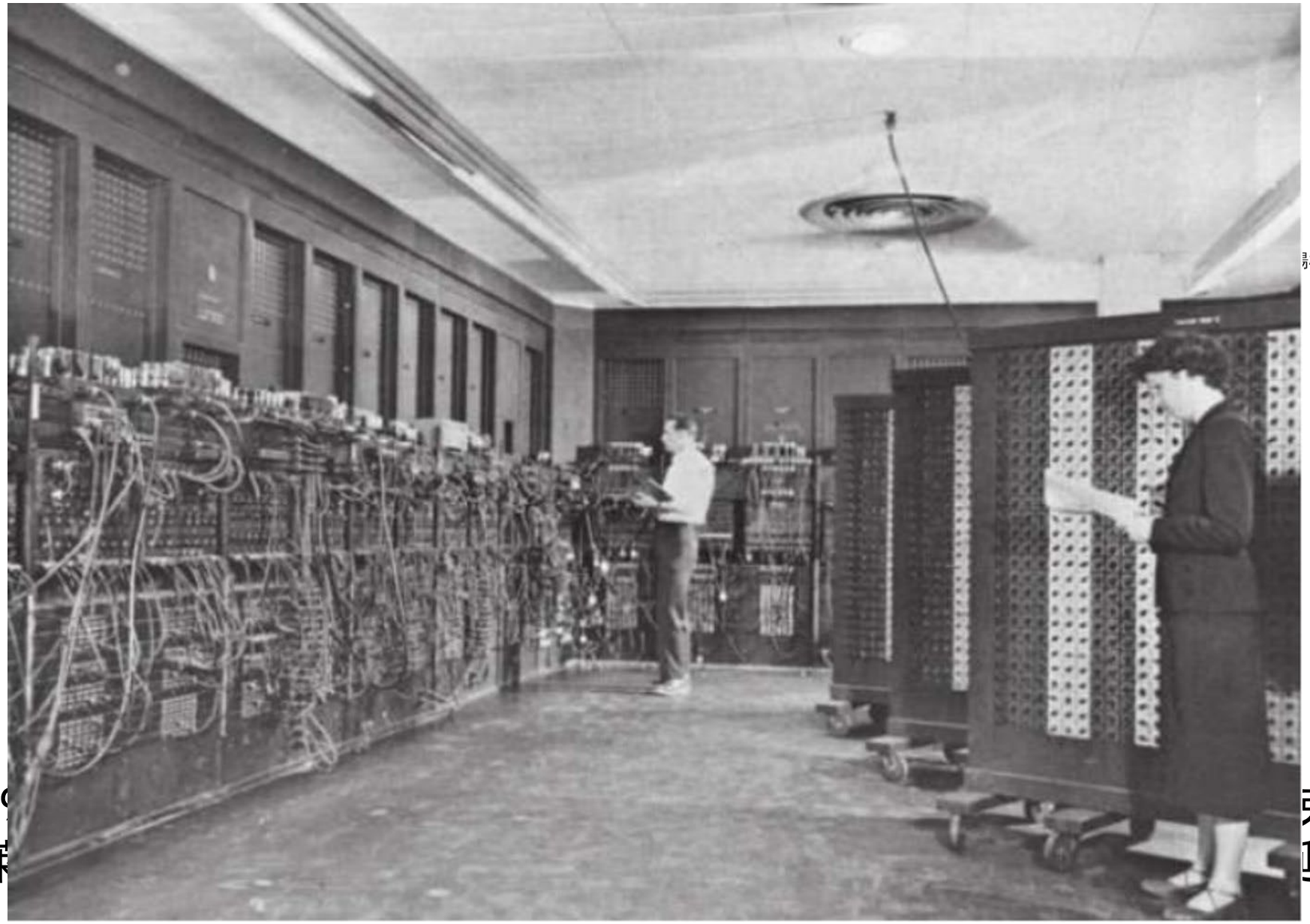


电子出现的概率

电子具有波动性

电子在原子核周围有的区域出现的多，有的区域出现的次数少，就像“云雾”笼罩在原子核周围，因此叫做电子云模型。电子云密度大的地方，表面电子在此地方出现的机会多；反之，出现的机会少

真空管计算机



陽極電流 I_A

19 弗
莱 生。

电子共有化运动

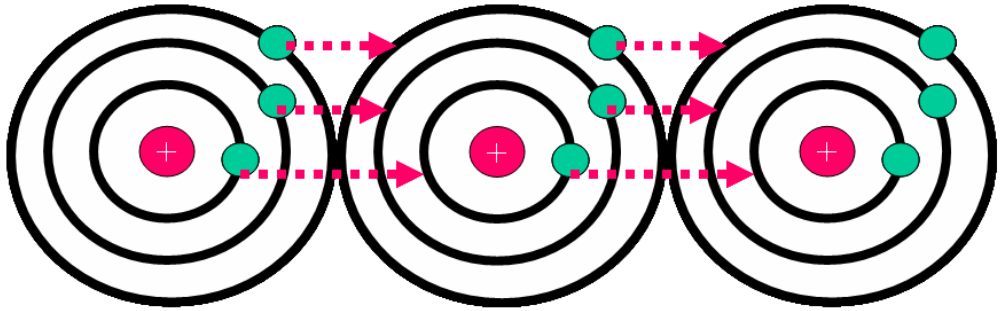
电子共有化运动：

原子组成晶体后，由于电子壳层的交叠，电子不再完全局限在某一个原子上，可以由一个原子转移到相邻的原子的相同电子轨道上去，因而，电子将可以在整个晶体中运动。这种运动称为电子的共有化运动。

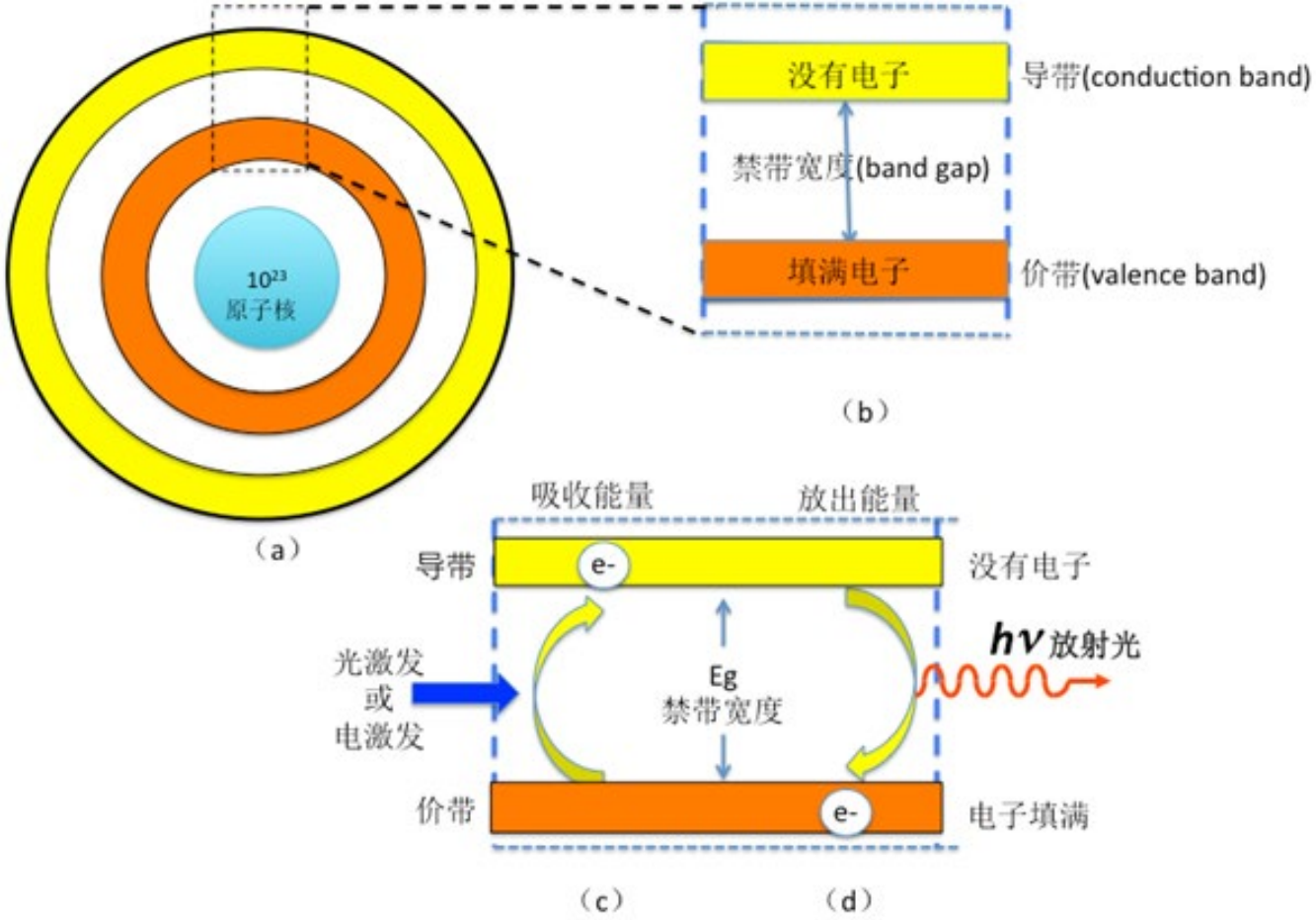
特点：

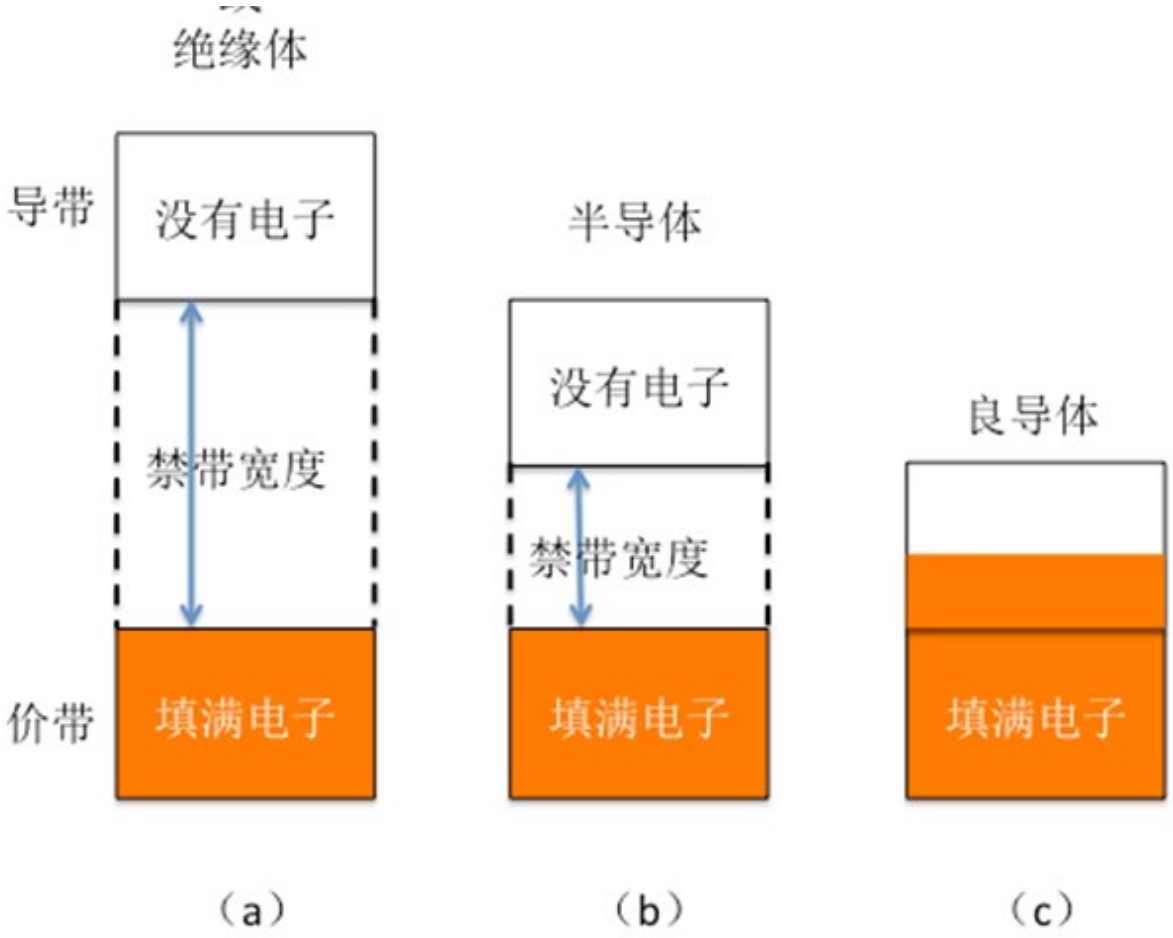
1.外层电子轨道重叠大，共有化运动显著。

2.电子只能在能量相同的轨道之间转移，引起相对应的共有化。



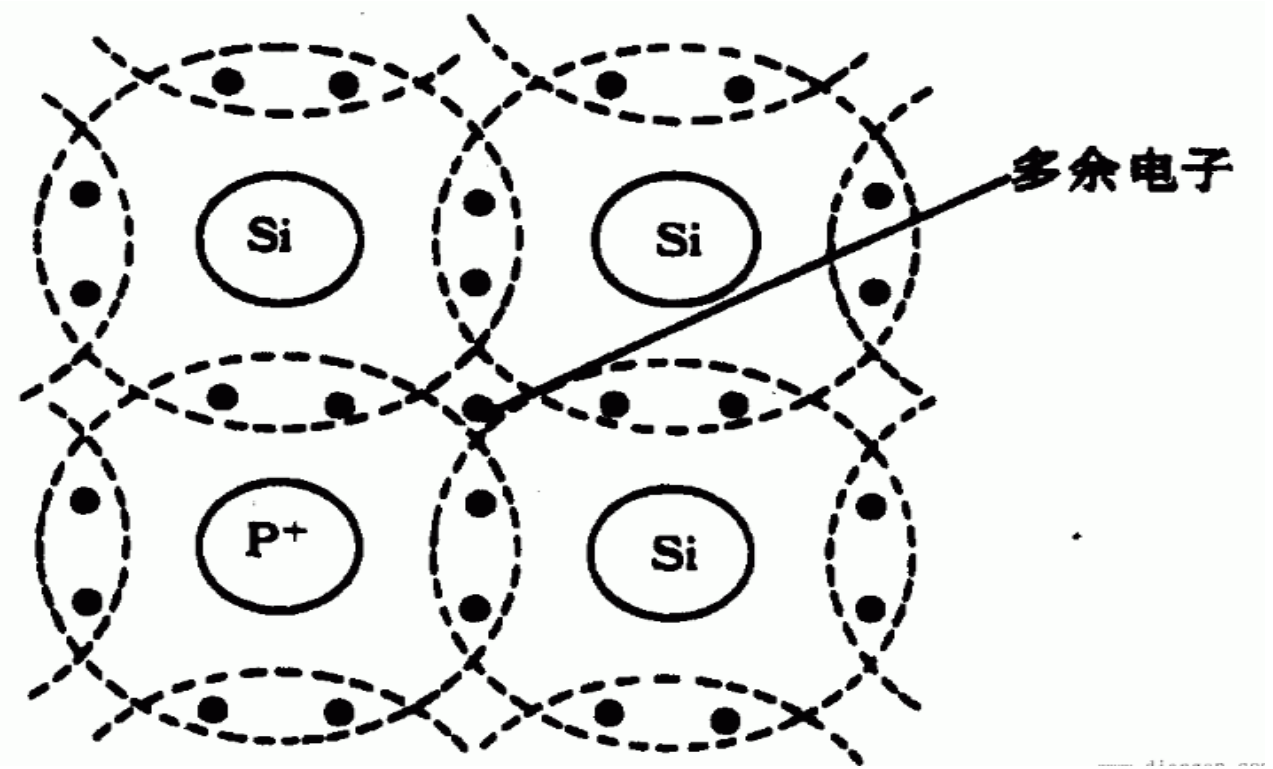
半导体中的电子状态和能带





施主杂质和施主能级

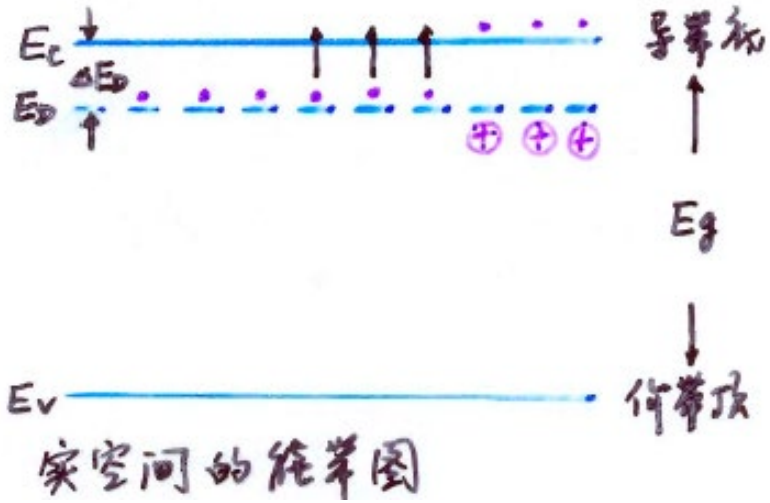
- 施主杂质
- 像V族元素在硅、锗中形成替位式杂质并且电离时能够释放电子而产生导电电子并形成正电中心，称此类杂质为施主杂质或n型杂质。



施主杂质和施主能级

施主电离：

1. 杂质能级用短线表示
   （分立能级，局域，未形成能带）



2. $\Delta E_D \ll E_g$

T=0K, 束缚态

T≠ $0K$,能带角度：电子从 E_D跃迁到E_c，成为导带电子。
空间角度：电子脱离 P^+ 离子的库伦束缚，运动到无穷远。

离化态

电离的原因：热激发，远红外光的照射。

$\Delta E_D \ll E_g$

施主杂质和施主能级

综上所述我们可以看出：

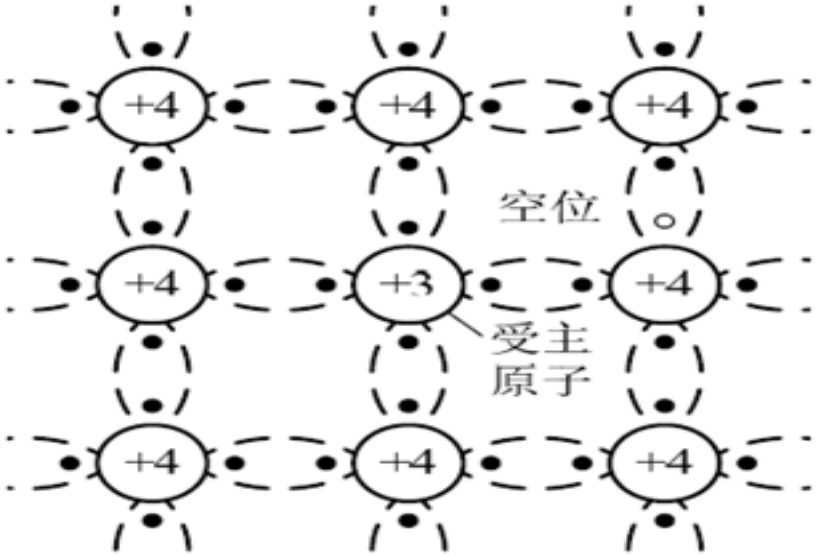
束缚在杂质原子的电子被激发至导带成为导电电子，该原子变成正电中心，该过程叫施主电离。这种杂质叫施主杂质。

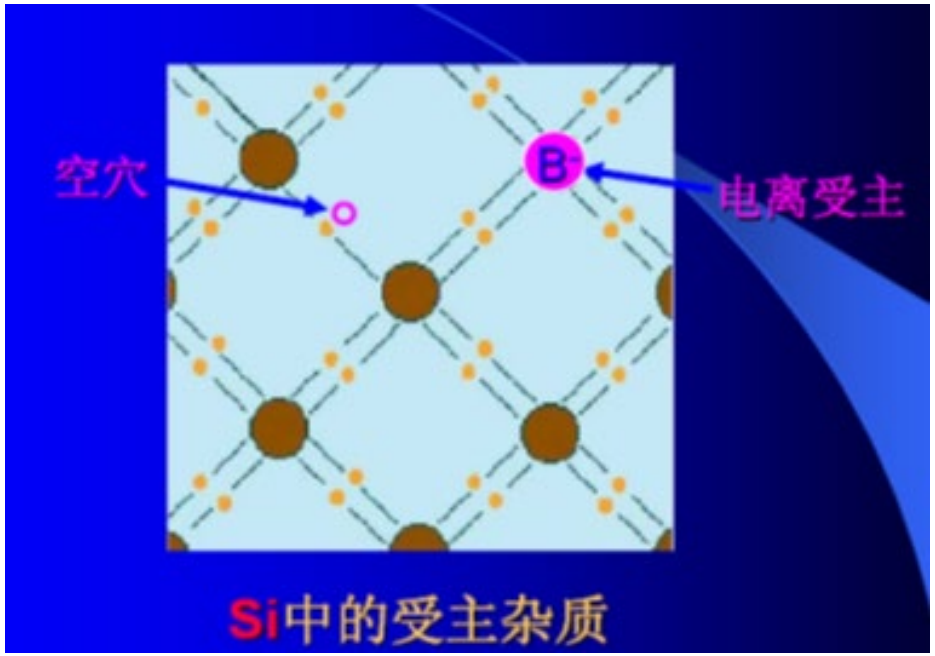
施主杂质：
- 束缚态：杂质未电离，中性。
- 离化态：电离后成为正电中心，　并释放电子。

- 杂质电离比本征激发容易得多。
- 施主杂质电离，导带电子增多。
- 主要靠电子导电的半导体叫n型半导体。

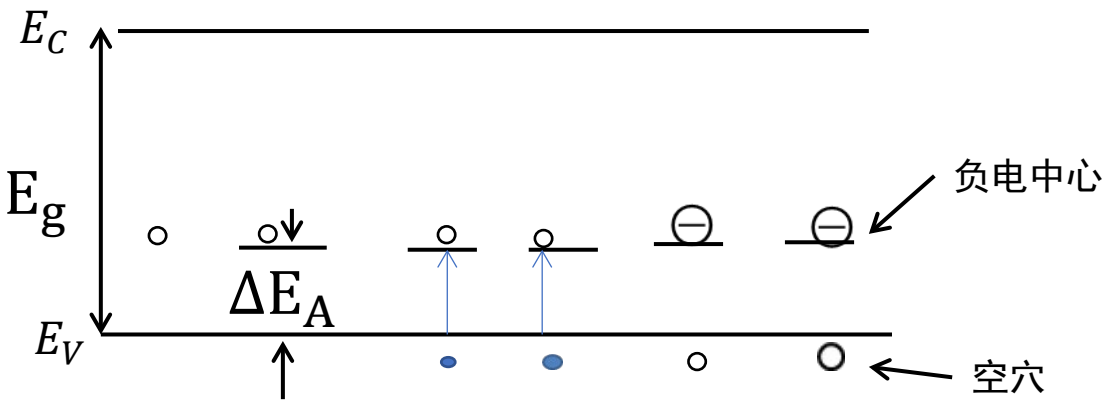
受主杂质和受主能级

- 受主杂质
- 像III族元素在硅、锗中形成替位式杂质并且电离时能够接受电子而产生导电空穴并形成负电中心，称此类杂质为受主杂质或p型杂质。





受主杂质和受主能级



受主杂质能级E_A：　被受主杂质束缚的空穴的能量状态。

注意：

1、能带图中表示空穴的能量越往下越高。

2、受主电离实际是电子从价带跃迁至E_A，价带中产生导电空穴。

受主杂质和受主能级

受主电离：

束缚在杂质能级的空穴被激发到价带成为价带空穴，该原子变为负电中心，这个过程叫做受主电离。

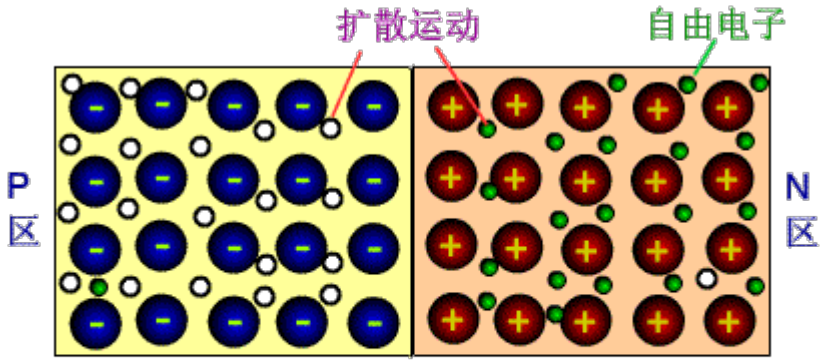
受主杂质电离能 $\Delta E_A \ll E_g$.

杂质电离结果，价带空穴增多。主要靠空穴导电的半导体叫p型半导体。

按杂质向半导体提供载流子的类型分类：

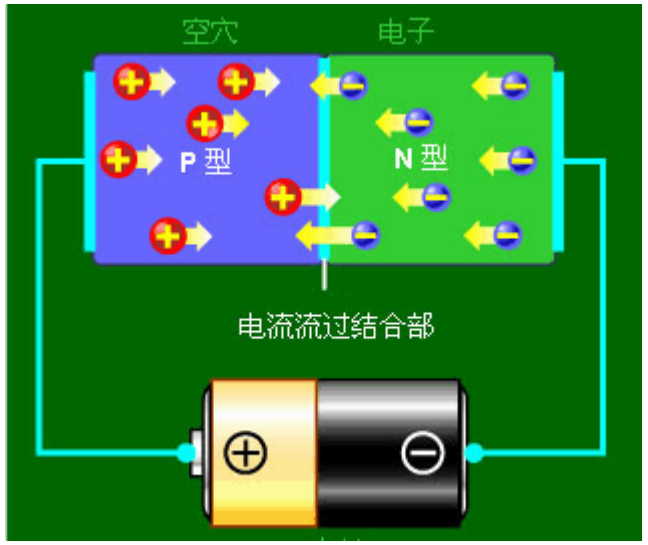
- N型半导体
- P型半导体
- 本征半导体

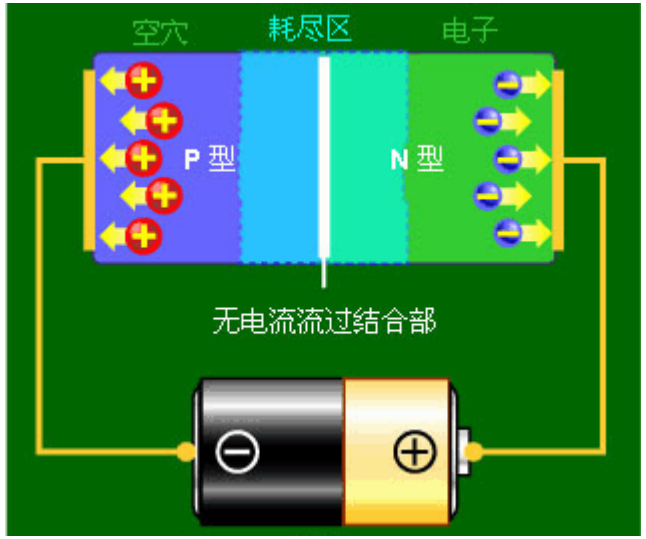
PN结及其整流特性



(a)P区与N区中载流子的扩散运动

PN结的形成





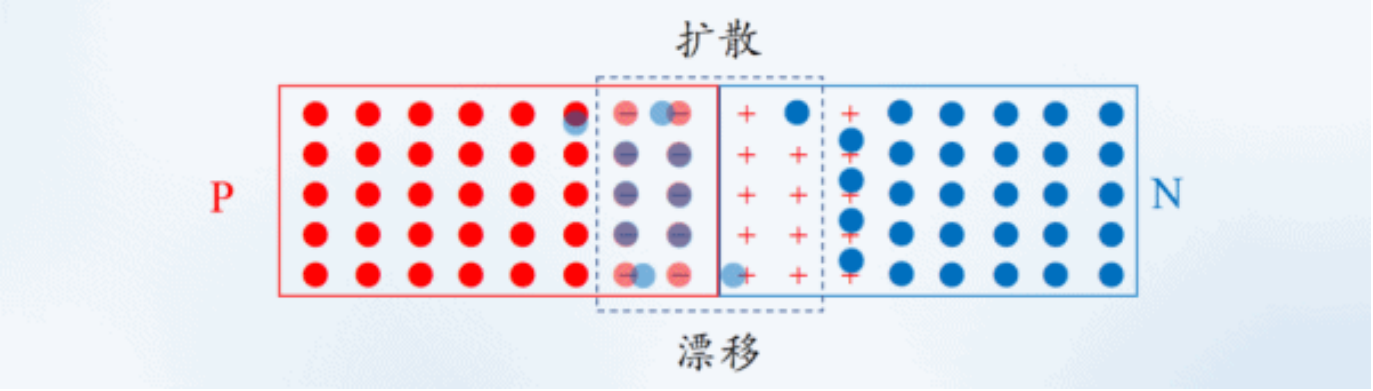
平衡p-n结特性

7.1.2空间电荷区

P–n结形成物理过程

开始因浓度差 ⇨ 引起多子扩散 ⇨ 产生空间电荷区

⇨ 出现内建电场 { 阻止多子扩散 / 利于少子漂移 } ⇨ 最终达动态平衡

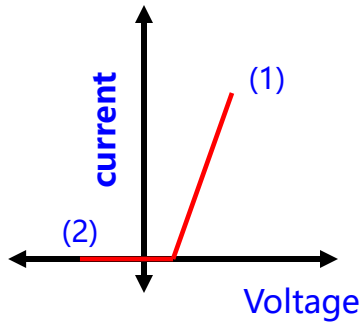


$$J_n = J_{n,diff} + J_{n,dr} = 0$$

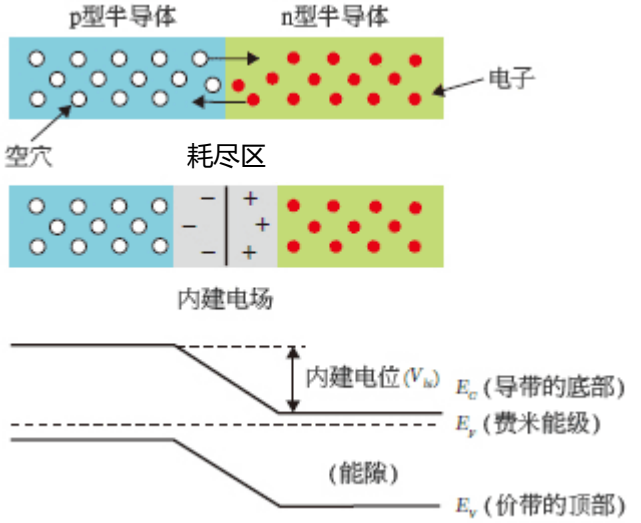
$$J_p = J_{p,diff} + J_{p,dr} = 0$$

平衡p-n结特性

PN Junction

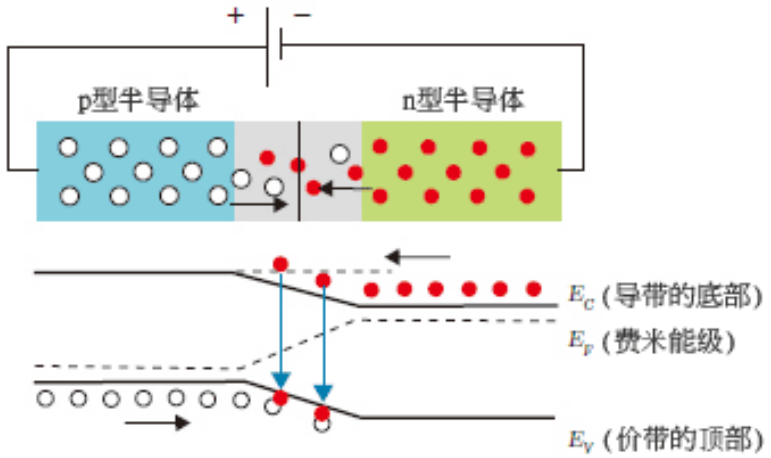


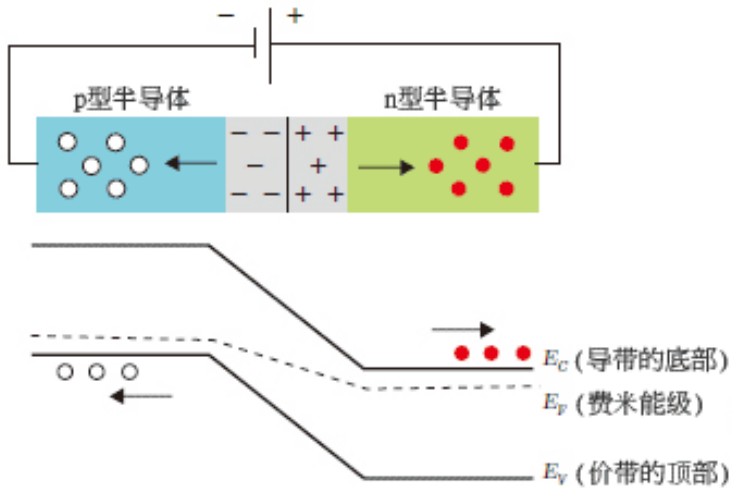
Diode



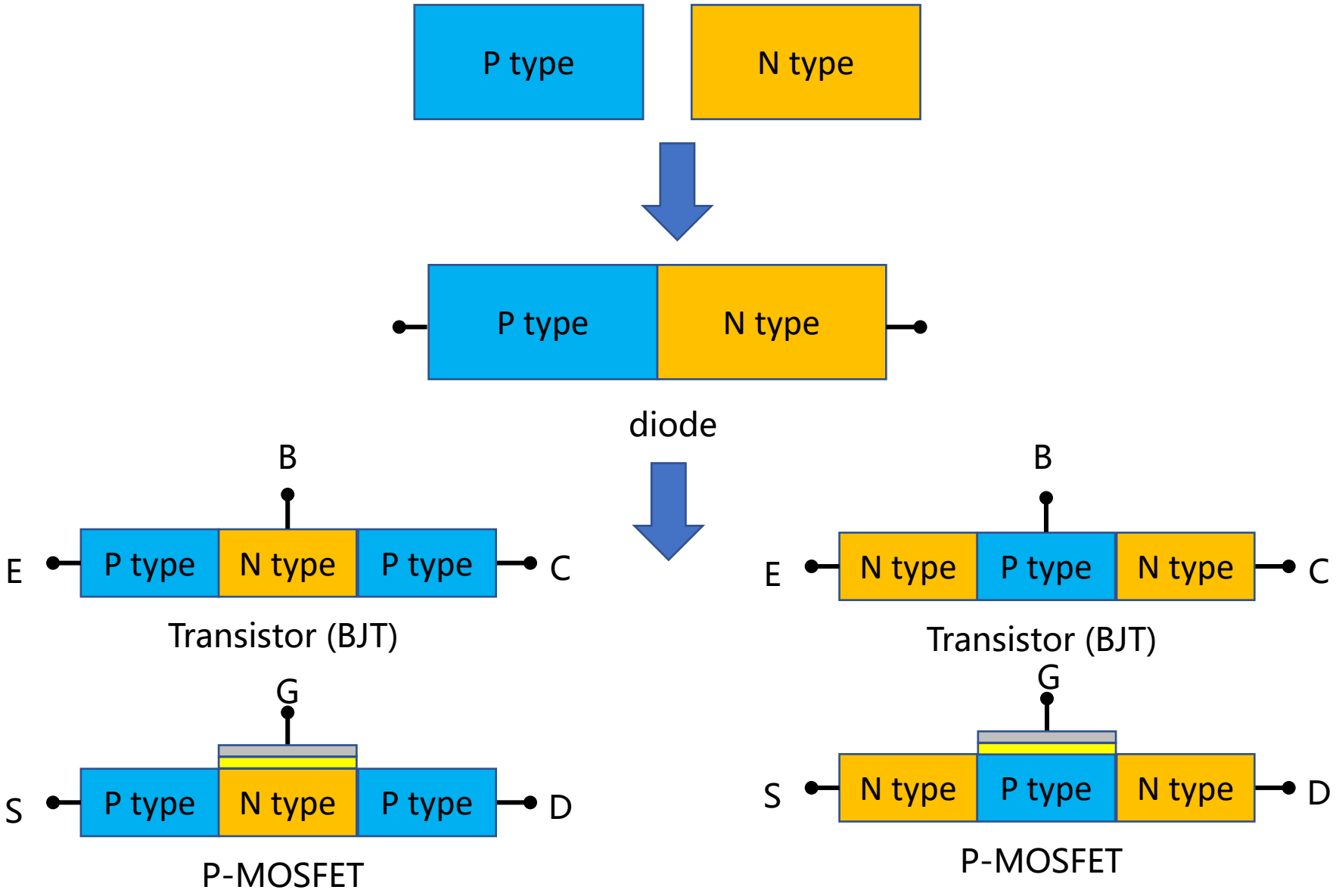
Reversed Bias

Forward Bias

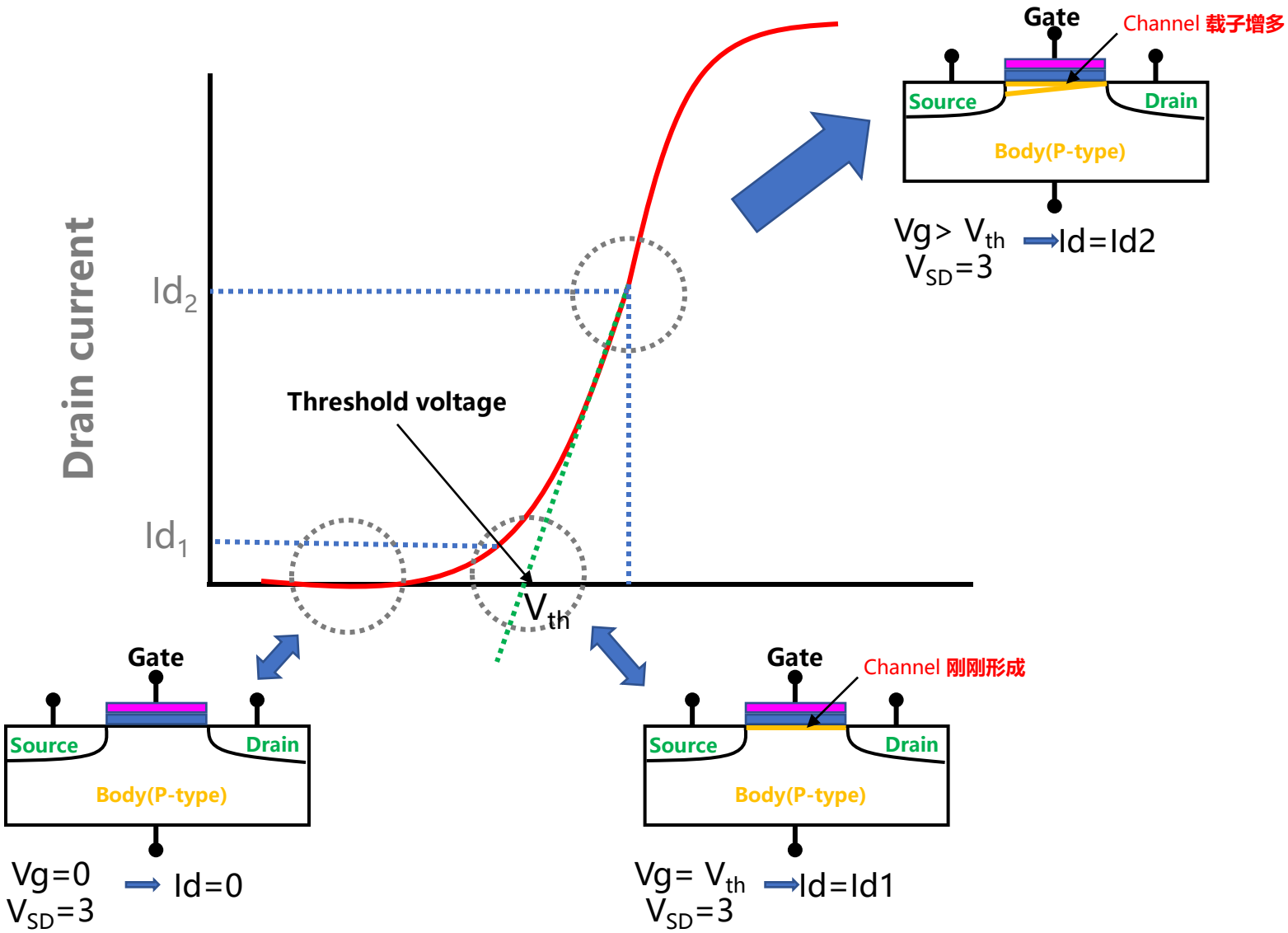




从二极管到三极管


P type
N type
P type
N type
diode
B
E
P type
N type
P type
C
Transistor (BJT)
B
E
N type
P type
N type
C
Transistor (BJT)
G
S
P type
N type
P type
D
P-MOSFET
G
S
N type
P type
N type
D
P-MOSFET

晶体管

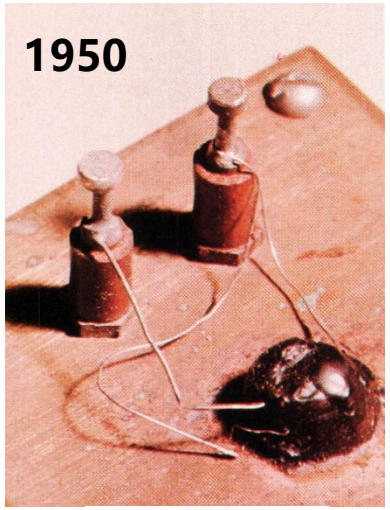

Drain current
Id2
Id1
Threshold voltage
Vth
Gate
Channel 载子增多
Source
Drain
Body(P-type)
Vg> Vth
VSD=3
Id=Id2
Gate
Source
Drain
Body(P-type)
Vg=0
VSD=3
Id=0
Gate
Channel 刚刚形成
Source
Drain
Body(P-type)
Vg= Vth
VSD=3
Id=Id1

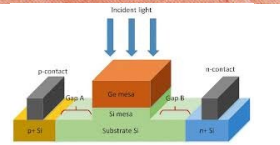
晶体管和集成电路的发明

First functional point contact solid state amplifier - Transistor based on Ge semiconductor at Bell lab

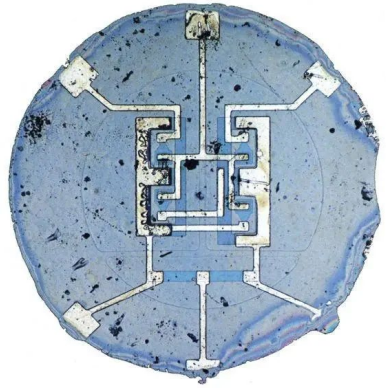
1947

Bell Labs semiconductor Group: Brattain, Bardeen, Shockley won Nobel Prize in 1956 lab





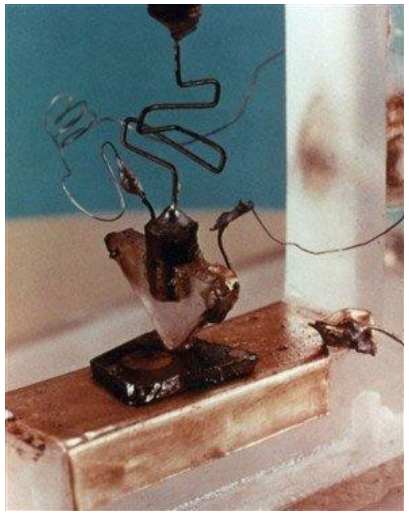
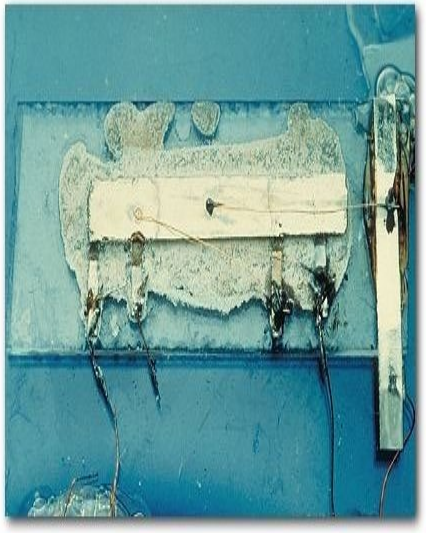
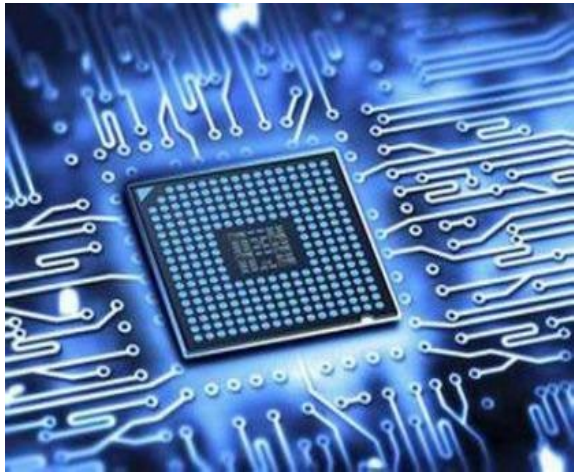
Ge Mesa(junction)



1960 Si Planar (MOSFET)

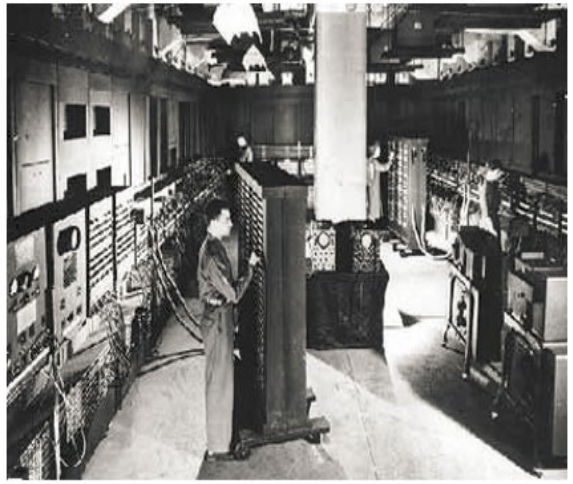
半导体发展简史

集成电路从产生到成熟大致经历了如下过程：**电子管——晶体管——集成电路——超大规模集成电路**

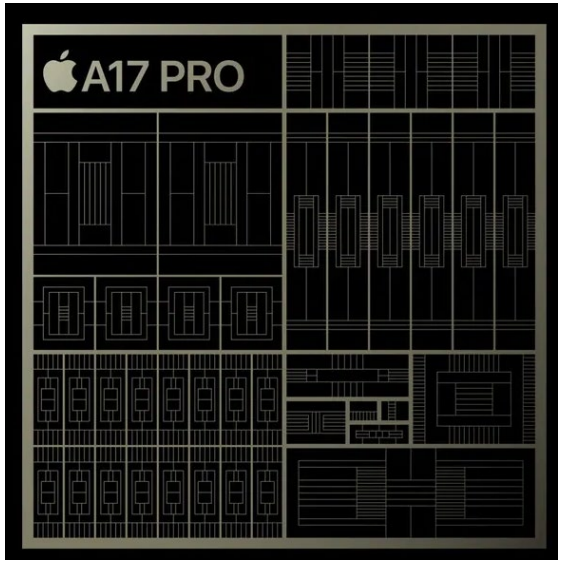




- 半导体晶体管和集成电路触发了第二次信息革命

半导体晶体管取代电子管：长途电话信号放大器、半导体收音机，电脑等



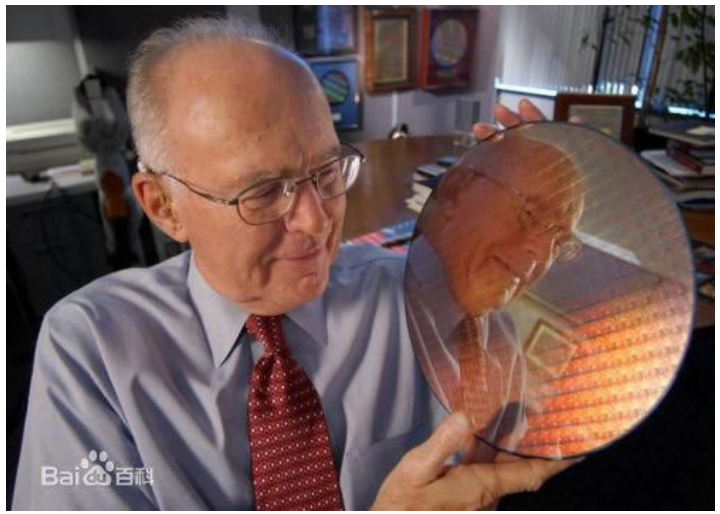
真空电子管：
体积大、能耗高、需预热等



苹果15 Pro手机
A17芯片（6核CPU，6核GPU）
3nm工艺， 190亿个晶体管， 35万亿次每秒 (3W)

摩尔定律

1963年，F.M Wanlass和C .T.Sah首次提出CMOS技术。
1965年戈登.摩尔提出摩尔定律，他预测硅芯片每隔18个月集成度就会翻一番。CMOS器件的发明有效的实践了摩尔定律。
1966年，美国贝尔实验室使用硅外延平面工艺制造成第一块公认的大规模集成电路。



戈登.摩尔

摩尔定律

如果汽车工业符合摩尔定律

如果汽车工业在过去按照摩尔定律发展40年（1965-2005）的话：

汽车的性能

-价格 → ~7 RMB /每台

-速度 → 40000 km/每小时

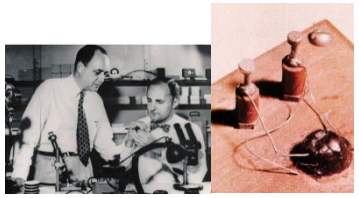
-油耗 → 1200 km/每升

-容量 → 400000 人/每台

The Most Exciting Discovery Period – Followed by the Skyrocketing Moore’ s Law Growth

Discovery of P-N junction R. Ohl

1940



The First Bipolar Junction Transistor (Ge base) M. Sparks, G. Teal

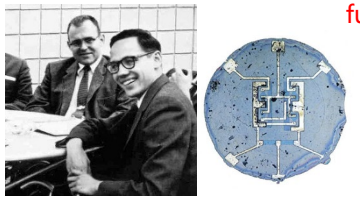
1951

Fairchild semiconductor Co started

1955

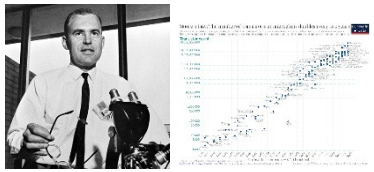
Invention of the "Planar" Manufacturing Process J. Hoerni

1959



First planar integrated circuit

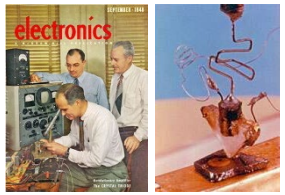
1960



“Moore’ s Law” predicts the future integrated circuits

1965

1947

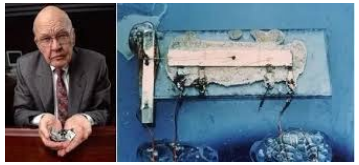


Point contact Transistor (Ge base) J, Bardeen, W. Brattain, W. Shockley

1954

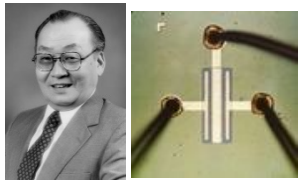
The first Si junction transistor M. Tanenbaum, C. Lee

1958



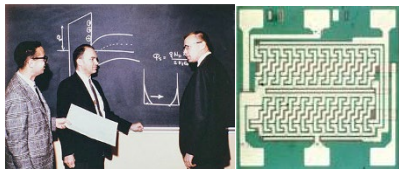
The First integrated Circuit (Ge base) J. Kilby H, R. Noyce, Fairchild

1960



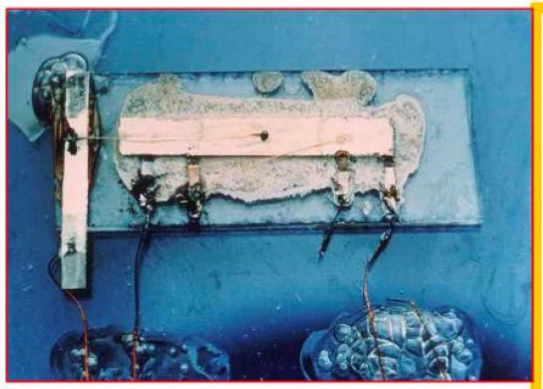
First field effect Transistor (MOS) J. Atalla, D. Khang

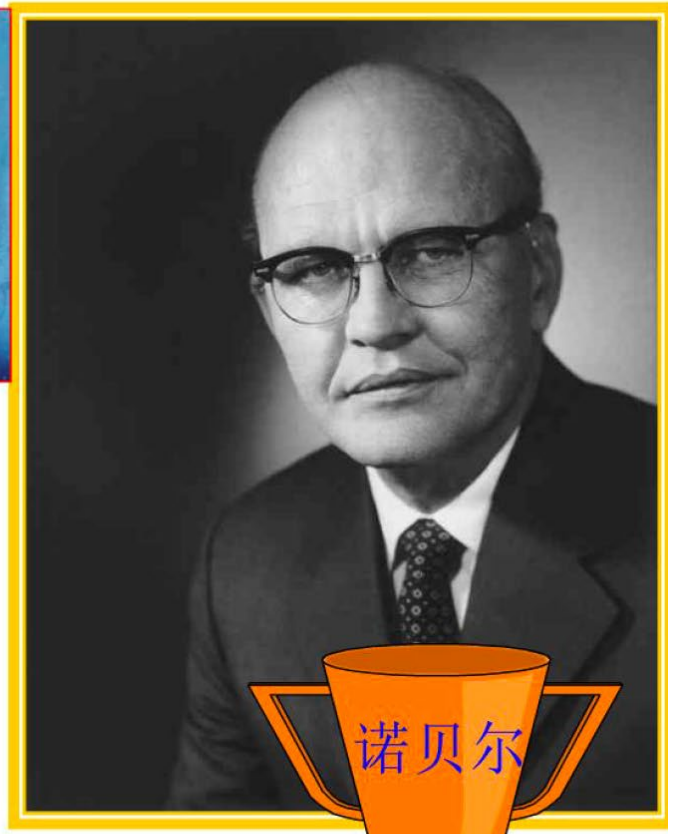
1964



集成电路

- 1958年：杰克-S-基尔比发明第一块集成电路

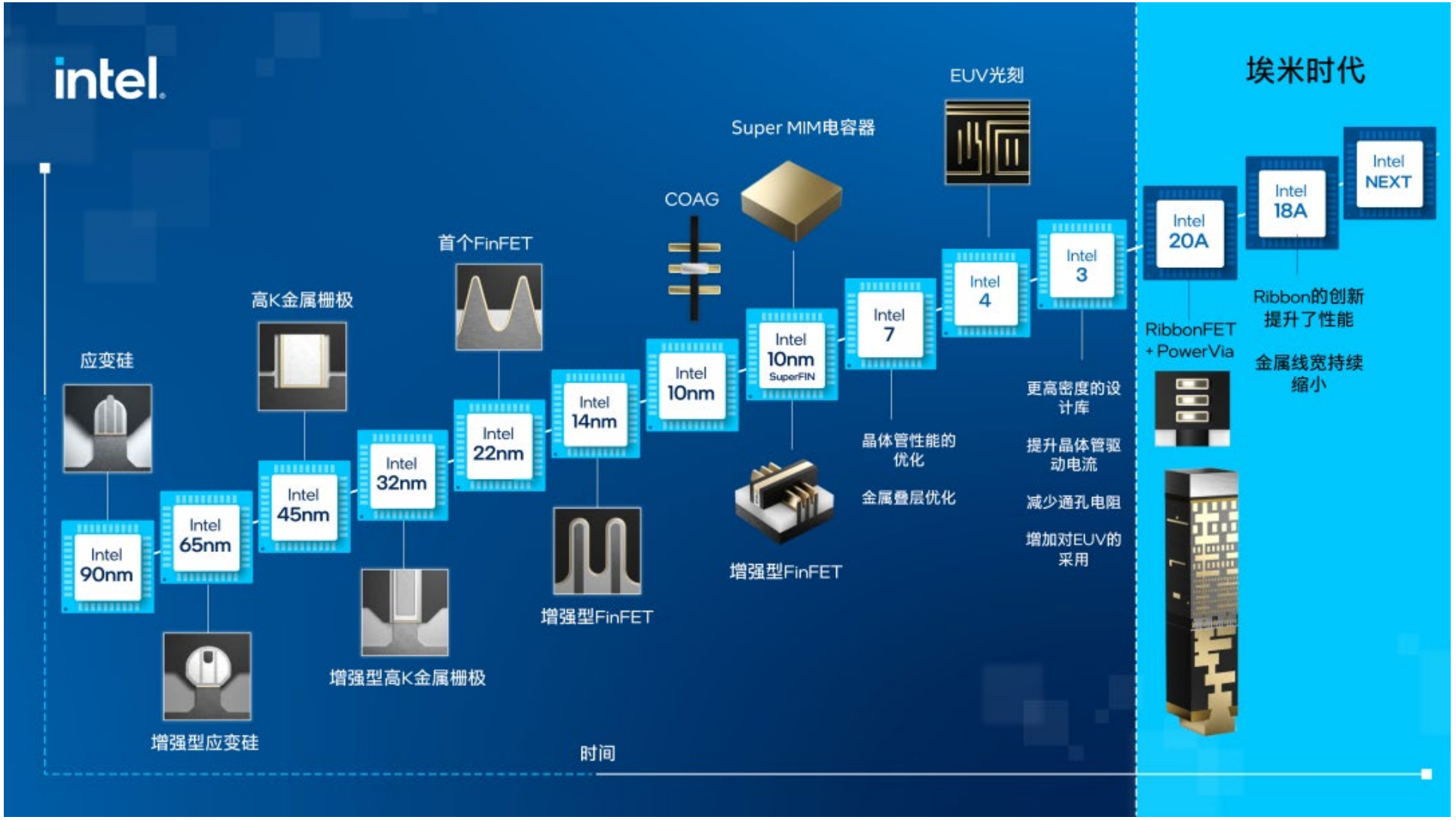




- 1966年：形成大规模集成电路
- 1971年: 英特尔公司研制出第一块CPU集成电路4004(4位)
- 1973年: 8008(8位)；
- 1978年: 8086(16位)；……

	SSI	MSI	LSI	VLSI	ULSI	GSI
元件数	$<10^2$	$10^2 \sim 10^3$	$10^3 \sim 10^5$	$10^5 \sim 10^7$	$10^7 \sim 10^9$	$>10^9$
门数	<10	$10 \sim 10^2$	$10^2 \sim 10^4$	$10^4 \sim 10^6$	$10^6 \sim 10^8$	$>10^8$

继续缩小，低功耗

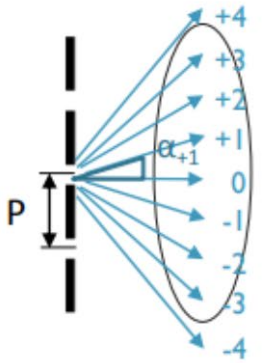

intel
应变硅
高K金属栅极
首个FinFET
COAG
Super MIM电容器
EUV光刻
埃米时代
Intel 90nm
Intel 65nm
Intel 45nm
Intel 32nm
Intel 22nm
Intel 14nm
Intel 10nm
Intel 10nm SuperFIN
Intel 7
Intel 4
Intel 3
Intel 20A
Intel 18A
Intel NEXT
增强型应变硅
增强型高K金属栅极
增强型FinFET
增强型FinFET
晶体管性能的优化
金属叠层优化
更高密度的设计库
提升晶体管驱动电流
减少通孔电阻
增加对EUV的采用
RibbonFET + PowerVia
Ribbon的创新提升了性能
金属线宽持续缩小
时间

光刻基础-衍射极限

the Rayleigh criterion:

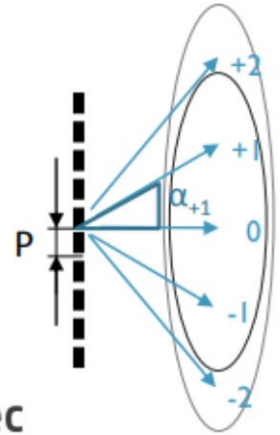
$$R\ (\text{smallest feature size}) = k1 * \lambda / NA$$

$$NA = n * \sin\alpha, \qquad k1 = 0.25$$



$\sin\alpha_n \downarrow = n\lambda/P \uparrow$

Large pitch → small α
Easy image formation, as many diffraction orders are captured by NA.



$\sin\alpha_n \uparrow = n\lambda/P \downarrow$

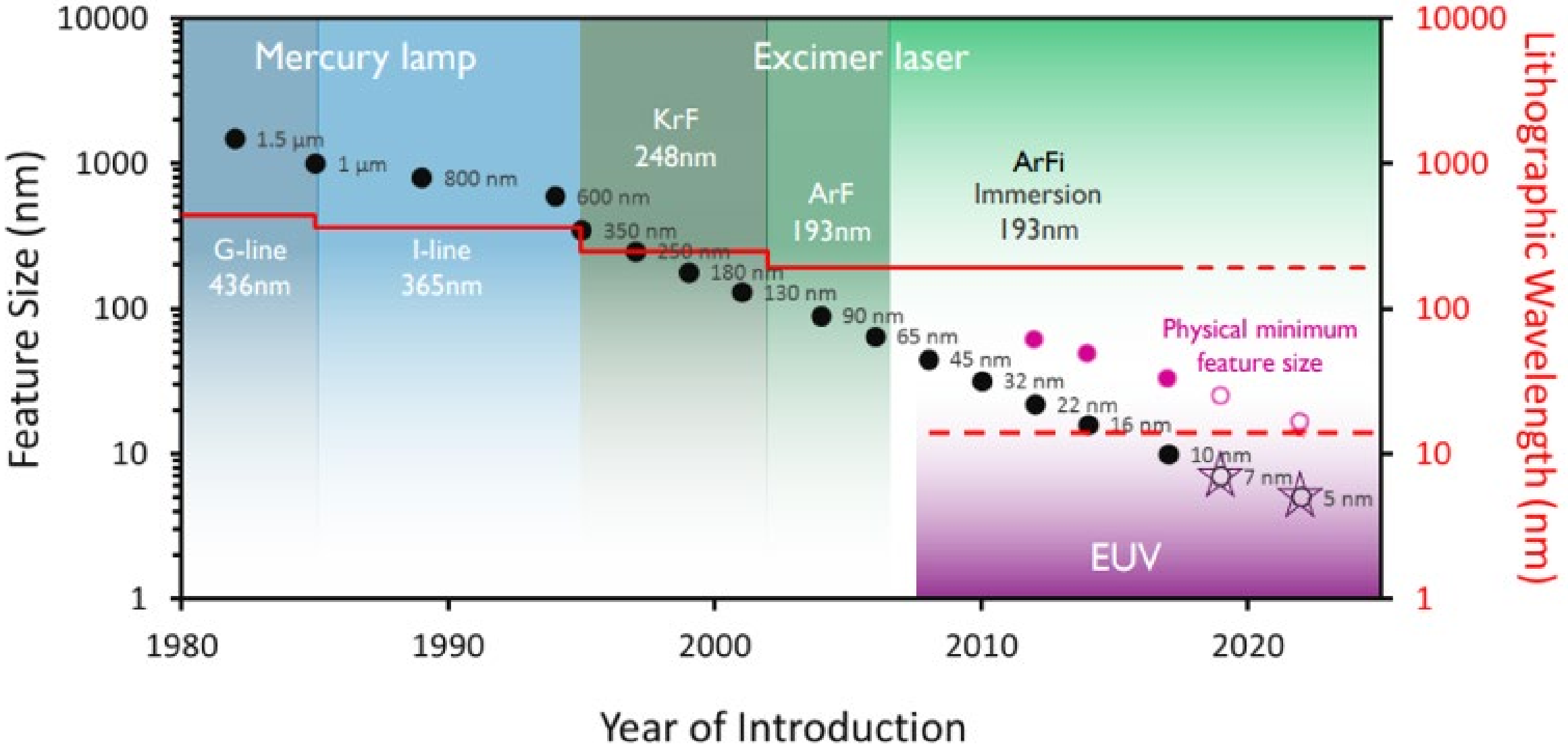
Small pitch → large α
Image formation requires at least 2 orders to be captured (e.g. 0 and +1).
Larger NA can help capturing more orders.

imec

PUBLIC KU LEUVEN

J. Microelectron. Manuf. **2**, 19020202 (2019)

光刻技术发展



J. Microelectron. Manuf. **2**, 19020202 (2019)

光刻机

ArFi (193nm)	EUV (13.5nm)
Transmission optics (lenses)	Reflection optics (Bragg mirrors)
Excimer laser source	Laser produced plasma source (LPP)
Immersion (NA_{water}=1.33)	Vacuum (NA= 0.33)

Figure 2. Comparison of an ASML ArF immersion scanner and an ASML EUV scanner. Courtesy of Vu Luong, IMEC[14].

1997, VNL

Extreme Ultraviolet Lithography

Imaging the Future

Livermore researchers are part of a collaboration between private industry and DOE laboratories dedicated to making extreme ultraviolet lithography the technology of choice for manufacturing the next generation of microcomputer chips.

TWENTY-FIVE years ago, the computing equivalent of today's laptop was a room full of computer hardware and a cartload of punch cards.

Since then, computers have become much more compact and increasingly powerful largely because of lithography, a basically photographic process that allows more and more features to be crammed onto a computer chip. Light is directed onto a mask—a sort of stencil of an integrated circuit pattern—and the image of that pattern is then projected onto a semiconductor wafer covered with light-sensitive photoresist. Creating circuits with smaller and smaller features has required using shorter and shorter wavelengths of light.

However, current lithography techniques have been pushed just about as far as they can go. They use light in the deep ultraviolet range—at about 248-nanometer wavelengths—to print 150- to 120-nanometer-size features on a chip. (A nanometer is a billionth of a meter.) In the next half dozen years, manufacturers plan to make chips with features measuring from 100 to 70 nanometers, using deep ultraviolet light of 193- and 157-nanometer wavelengths. Beyond that point, smaller features require wavelengths in the extreme ultraviolet (EUV) range. Light at these wavelengths is absorbed instead of transmitted by conventional lenses. The result: no light, no image, no circuit.

Semiconductor manufacturers are, therefore, at a critical juncture. Soon, they must decide which lithographic horse to back in the race to the next generation of microchip manufacturing. There are currently four possible alternatives: EUV, x-ray, electron-beam, and ion-beam lithography.

Creating a Virtual Laboratory

Two years ago, three Department of Energy national laboratories—Lawrence Livermore, Lawrence Berkeley, and Sandia/California—formed the Virtual National Laboratory (VNL) to research and develop extreme ultraviolet lithography (EUVL) technology. The VNL is funded by the Extreme Ultraviolet Limited Liability Company—a consortium of Intel Corporation, Motorola Corporation, Advanced Micro Devices Corporation, and Micron Technology, Incorporated—in one of the largest cooperative research and development agreements within the Department of Energy. The three-year, $250-million venture is dedicated to developing the EUVL technology for commercial manufacturing of computer chips and to move this technology into production facilities in the first decade of the 21st century.

Each national laboratory brings unique contributions to this effort. Lawrence Livermore supplies its expertise in optics, precision engineering, and multilayer coatings. Sandia provides systems engineering, the photoactive polymer thin film exposed by the light, and the light source. Berkeley contributes its Advanced Light Source capability to generate EUV light to characterize optics and resists at the nanometer scale.

The VNL's lithography system uses mirrors to project the image of a reflective mask onto the photoresist-coated semiconductor wafer. Ultimately, this system will enable a microchip to be manufactured with etched circuit lines smaller than 100 nanometers in width, extendable to below 30 nanometers. The resulting microprocessors would be a hundred times more powerful than those made today. Memory chips would be able to store a thousand times more information than at present.

"Lithography is generally viewed as the enabling technology for each new generation of semiconductor devices," says Don Sweeney, Lawrence Livermore's program manager for EUVL. "To put this technology into production facilities in 10 years, we need to show that the technology can work under real manufacturing conditions."

The VNL's current focus is on building and integrating the necessary

What's at Stake

> . . . [T]he first 30 years of the integrated circuit had from two to five times the impact on the U.S. economy as the first 30 years of the railroad. Or, to put it another way, the transformation of the nineteenth century U.S. economy by the railroad took 60 years to achieve half the effect that microelectronics had over 30 years.
>
> —Kenneth Flamm
> "More for Less: The Economic Impact of Semiconductors"
> December 1997

Semiconductors are ubiquitous in our lives. They are found in our cars, televisions, radios, telephones, stereos, personal computers, children's toys—even dishwashers and ovens. According to research conducted by the Semiconductor Industry Association and the World Bank, each person worldwide uses on the average about ten million transistors in a lifetime, with this consumption increasing 55 percent each year. By the year 2008, projections are that each person will consume a billion transistors.

It's no wonder then that the annual sale of semiconductors worldwide will soon reach about one trillion dollars—the equivalent of the gross national product of the United States. Furthermore, it's no wonder that the next generation of lithographic technology—which is seen as the "gating technology" to the next generation of integrated circuits—is of such great interest to semiconductor manufacturers throughout the world.

1997, VNL

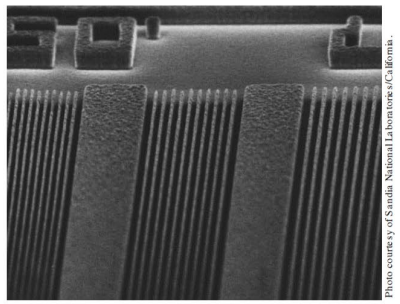
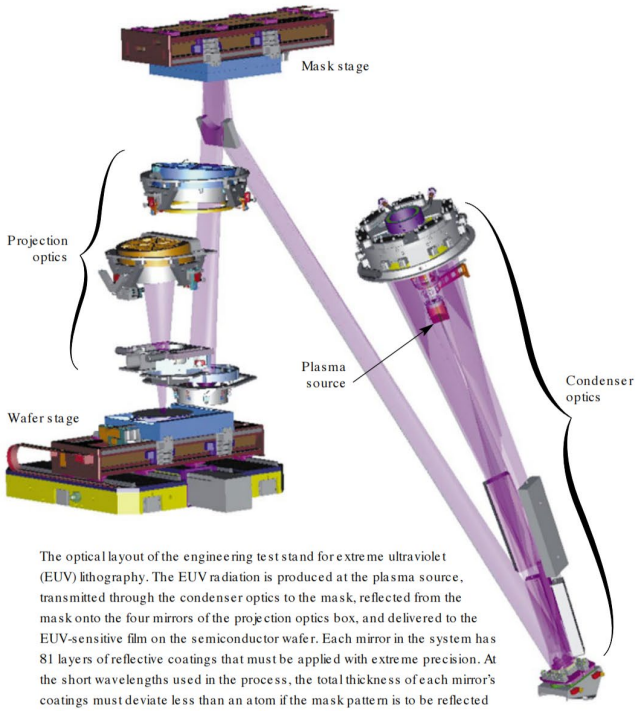


Photo courtesy of Sandia National Laboratories/California.

Using a prototype system, the Virtual National Laboratory has successfully printed lines as small as 50 nanometers (billionths of a meter) wide in photoresist. Current lithographic tools used in the semiconductor industry print patterns with 180-nanometer-size features.



The optical layout of the engineering test stand for extreme ultraviolet (EUV) lithography. The EUV radiation is produced at the plasma source, transmitted through the condenser optics to the mask, reflected from the mask onto the four mirrors of the projection optics box, and delivered to the EUV-sensitive film on the semiconductor wafer. Each mirror in the system has 81 layers of reflective coatings that must be applied with extreme precision. At the short wavelengths used in the process, the total thickness of each mirror's coatings must deviate less than an atom if the mask pattern is to be reflected without distortion. One such mirror is shown on p. 4.

technologies into an engineering test stand (ETS). Each national laboratory spearheads specific development areas for the ETS and for the systems beyond. Lawrence Livermore is leading the efforts to develop the optical systems and components, thin films, masks, and submicrometer metrology required for EUVL.

Brighter Light Is Key

The ETS (see the box on p. 7) includes a condenser optics box and a projection optics box. Both boxes house complex optical trains of precision concave and convex aspherical mirrors.

The main role of the condenser optics box is to bring light to the reflective pattern on the mask. "We want to bring as much light to the mask and, ultimately, the wafer, as possible," explains Sweeney. "The more light we deliver, the shorter the exposure time. It's like taking a picture with a camera. A picture taken in bright noonday sun requires a shorter exposure time than does a picture of the same scene taken at twilight."

For the semiconductor industry, brighter EUV images mean shorter exposure times, which translate to manufacturing more chips at a faster rate. The optics design team from Lawrence Livermore and Sandia designed a condenser optics system that collects and transports a significant fraction of the EUV light from the source to the reflective mask.

Once the image is reflected from the mask, it travels through the projection optics system. According to Sweeney, the projection optics box is the optical heart of the lithographic exposure system. "It is to the system what an engine is to a car," he explains. The four mirrors of the ETS projection optics system reduce the image and form it onto the wafer. "Again, imagine using a pocket camera. The camera lens transmits an image to the film, which—like the wafer—has a light-sensitive surface," says Sweeney.

small defect ends up being replicated, or printed, in the lithography process onto the computer chips being manufactured, thus damaging the chips' complex circuitry. A key breakthrough in this area was the development of an Ultra Clean Ion Beam Sputter Deposition System about two years ago. This system—also an R&D 100 Award winner—produces precise, uniform, highly reflective masks with fewer defects than those produced by

conventi
processe
p. 8.) In
significa
sputterir
operatio
now cor
0.1 defe
a factor-
densities
In fac
conditio
0.04 mec
during a

The Ultra
Sputter D
develope
Livermore
precise, u
reflective
requirem
generatio
is that it p
defect-fre
system co
than 0.1 c
centimete
The ultim
ultraviole
no more than 0.001 defects per square centimeter to a finished wafer blank.

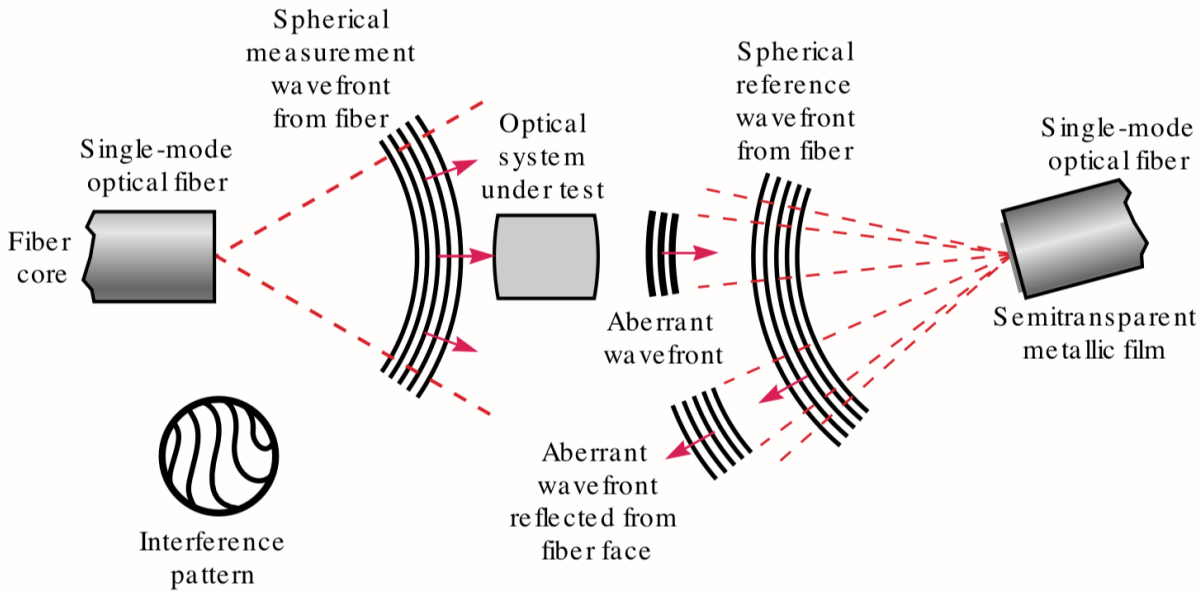
used in industry—up from 150-millimeter wafers. The ability to process larger wafers for mask substrates means both that the technology is working with industry standards and that patterns for larger chips can be placed on the wafer.

The Lawrence Livermore team has also conducted groundbreaking experiments looking at the propagation of defects during multilayer film growth. All masks have defects of some kind—some more, some less. First of all, there

leader for mask blank development. "We finally conducted experiments that are setting the lower bound of critical defect size."

The group has also made strides in repair strategies for mask defects. "One mask can cost tens of thousands of dollars," notes Burkhart. "When possible, repairing the defects saves the industry a lot of money."

Measuring at the Atomic Level



Schematic of the phase-shifting diffraction interferometer which uses two single-mode optical fibers. In this example, the interferometer is testing a lens, but the setup is similar for testing mirrors.

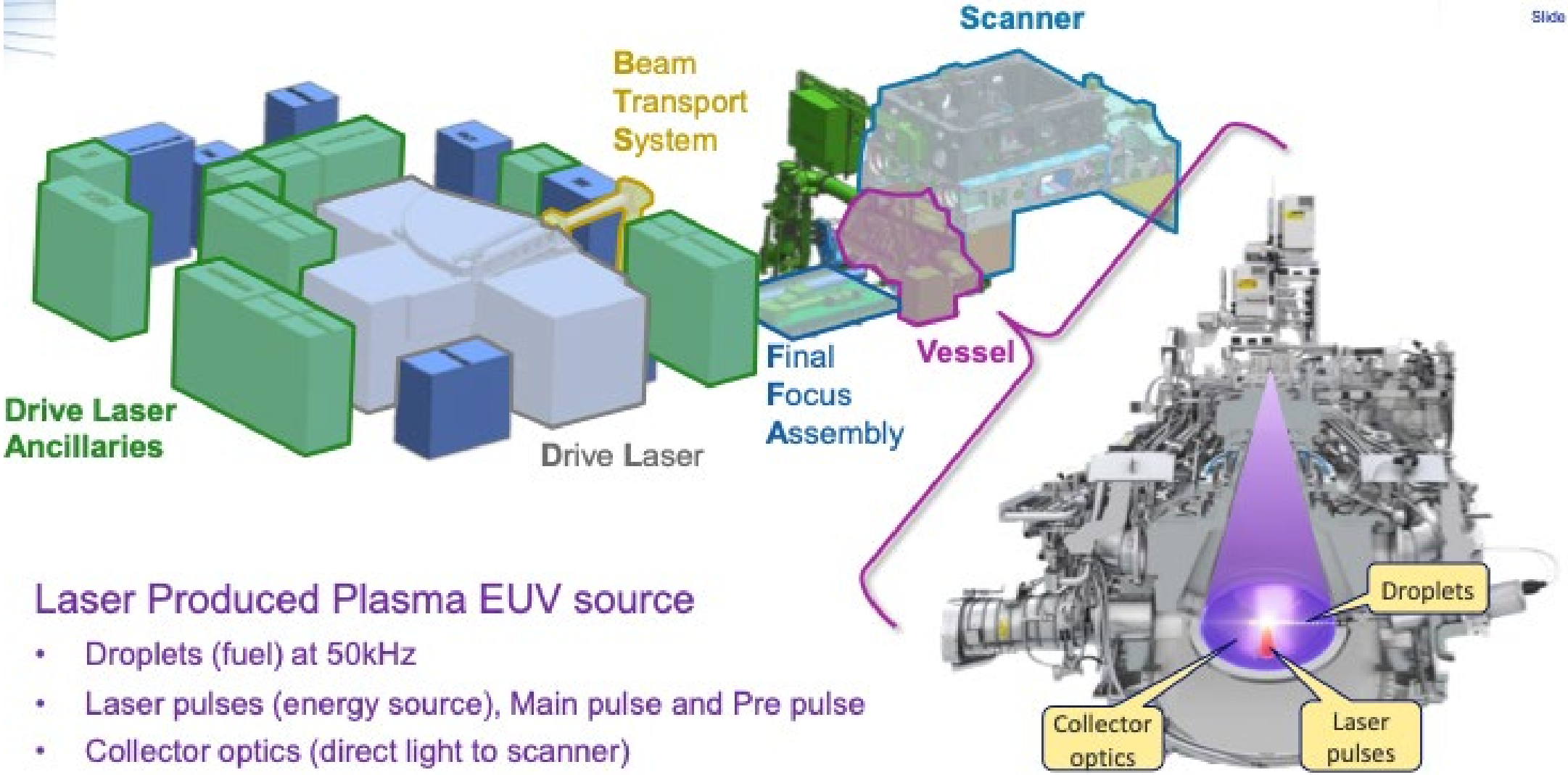
Lawrence Livermore National Laboratory

LPP

Introduction to the NXE EUV source

ASML

Slide 16



Laser Produced Plasma EUV source

- Droplets (fuel) at 50kHz
- Laser pulses (energy source), Main pulse and Pre pulse
- Collector optics (direct light to scanner)

Public

LPP

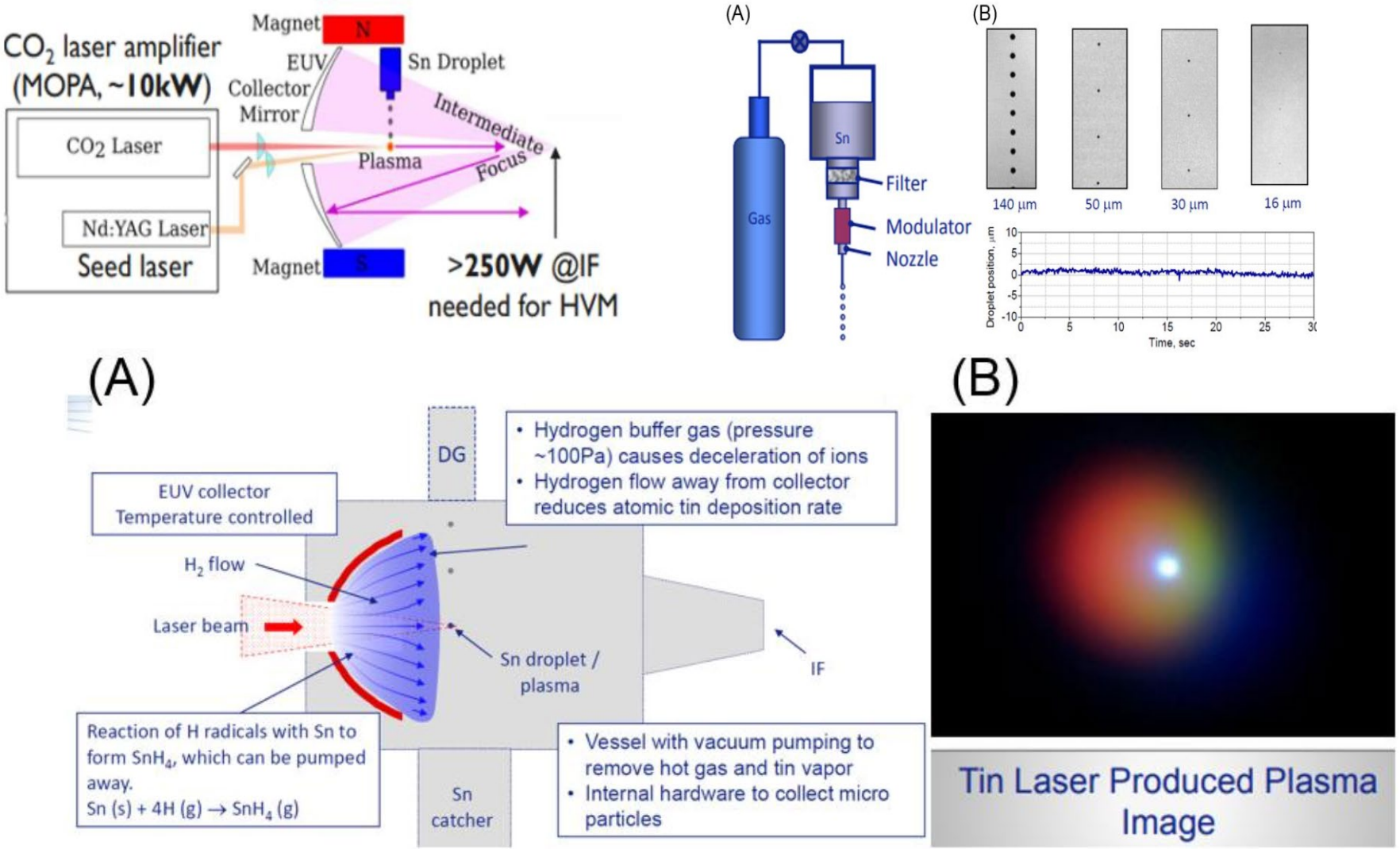
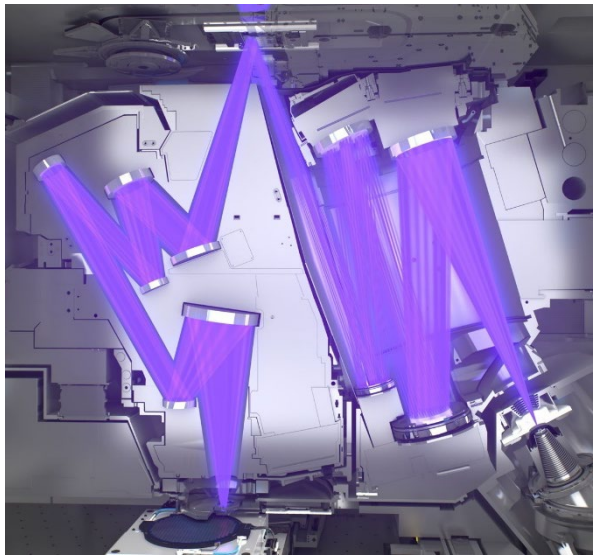
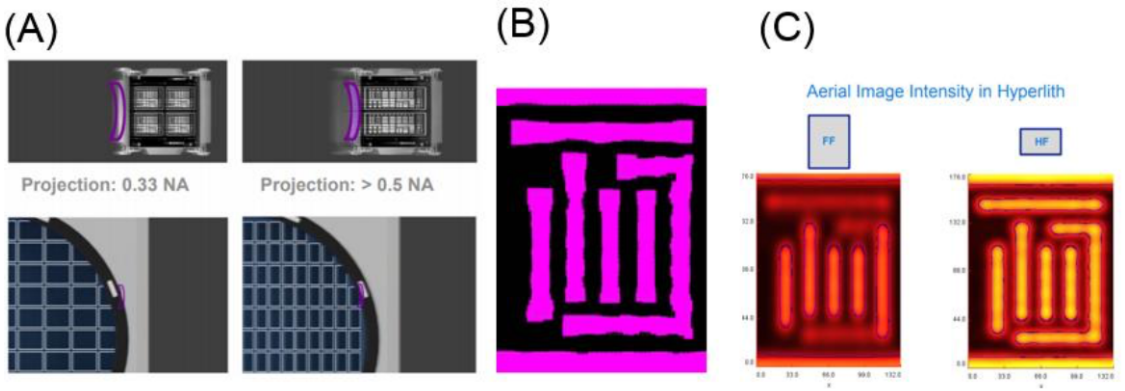


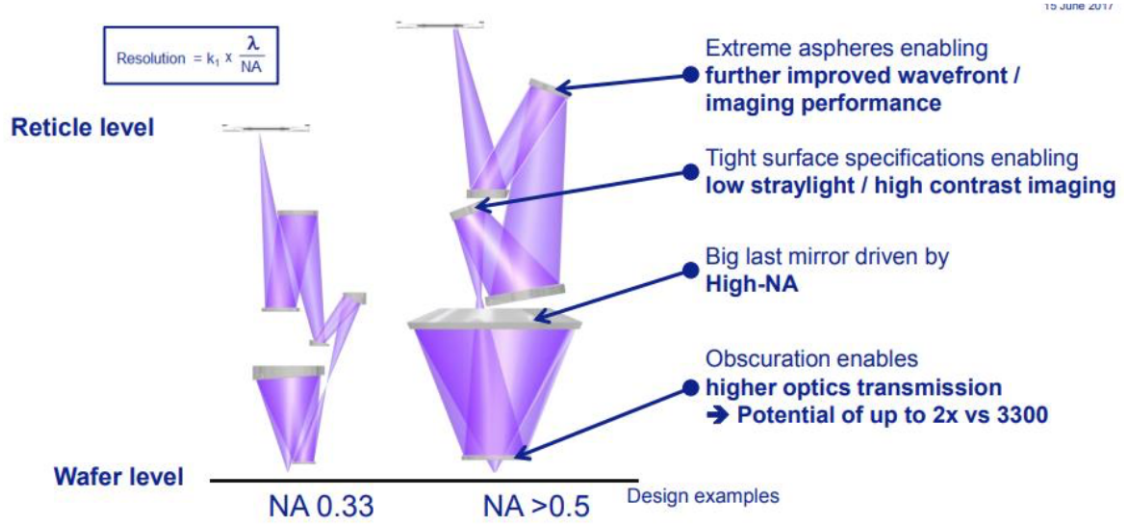
Figure 4. (A) Illustration of EUV light source vessel with hydrogen gas as buffer. (B) An image of laser produced plasma around a tin droplet[21]. Courtesy of Igor Fomenkov, ASML.

EUVL



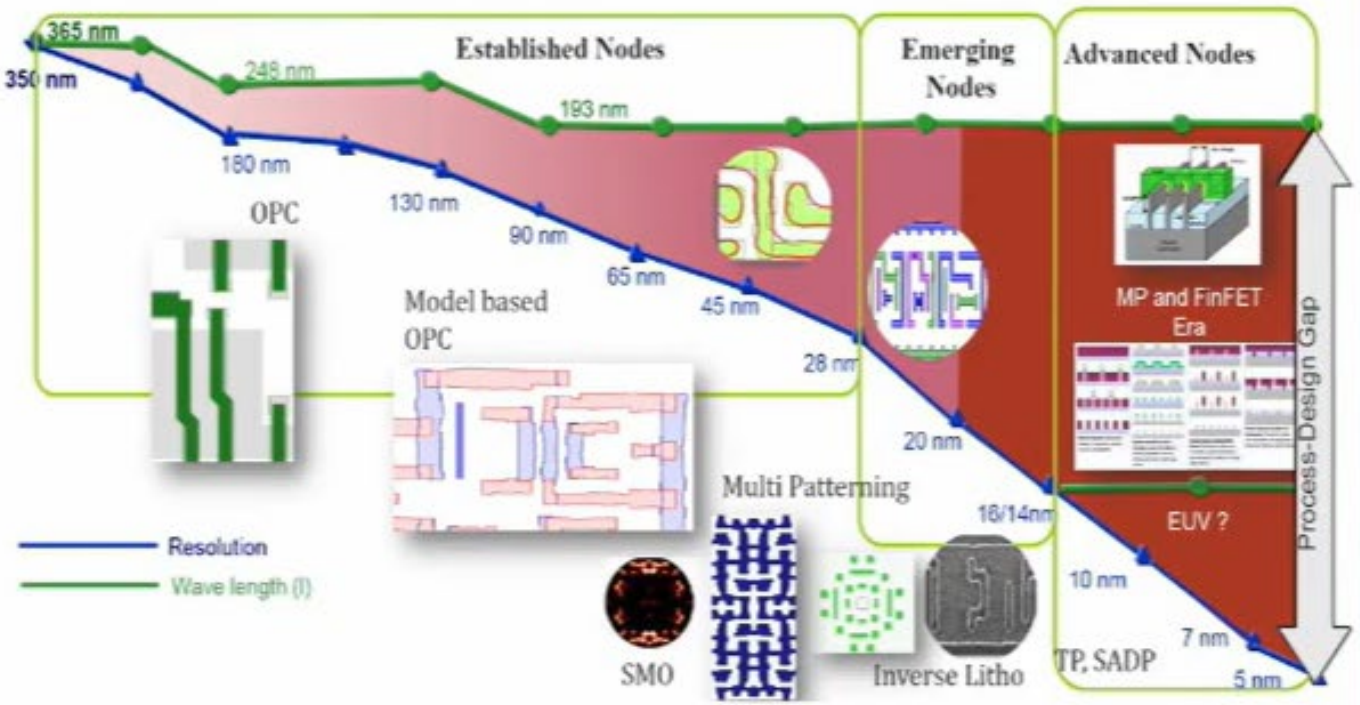


. (A) Anamorphic half field (HF) exposure with high NA compared with full field (FF) with 0.33 NA vs aerial image intensity mapping beteen FF and HF A from a test mask feature (B), where HF present gher contrast[28]. Courtesy of Jan van Schoot, ASML.



0. EUV reflection comparison between NA=0.33 and high NA mirrors[26]. Courtesy of Anthony Yen

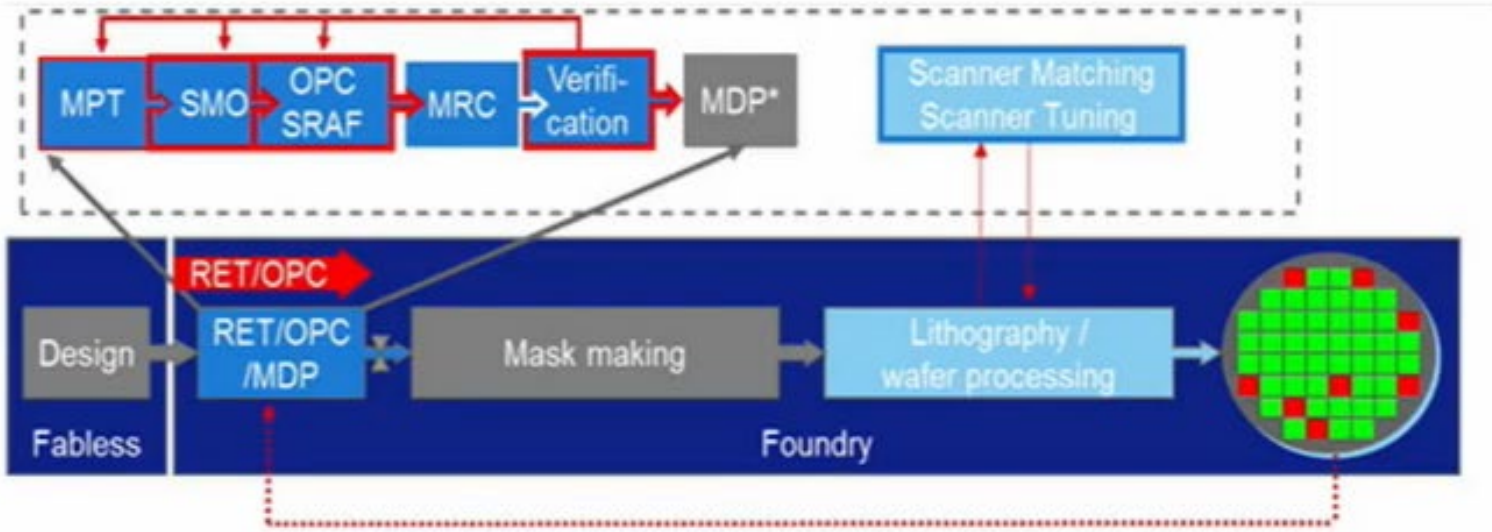
计算光刻



	32nm	28nm	22nm	14nm	10nm	7nm
Year	2009	2011	2011	2013	2017	202
Scanner	193	193/193i	193i	193i	193i	193
CDU	2.1nm	2nm	1.8nm	1.7nm	1.4nm	1.3n
Resolution	50nm	45nm	40nm	32nm	22nm	20n
Pitch	100nm	90nm	80nm	64nm	44nm	40n
Overlay	10nm	9nm	8nm	5nm	4.5nm	3.5n

- 工艺技术节点不段发展，对**光刻性能指标**要求越来越严格
- 从90nm工艺技术节点开始，**计算光刻技术**被公认为是进一步突破光学衍射极限以实现超强光刻分辨率的最有效的手段之一

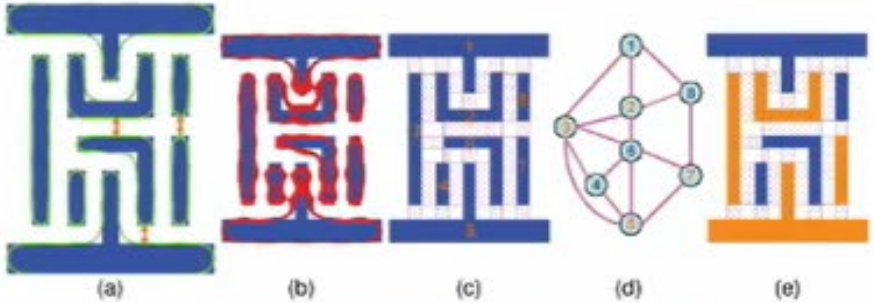
计算光刻



MDP – Mask data preparation
RET – Resolution enhancement technology
MPT – Multi patterning technology

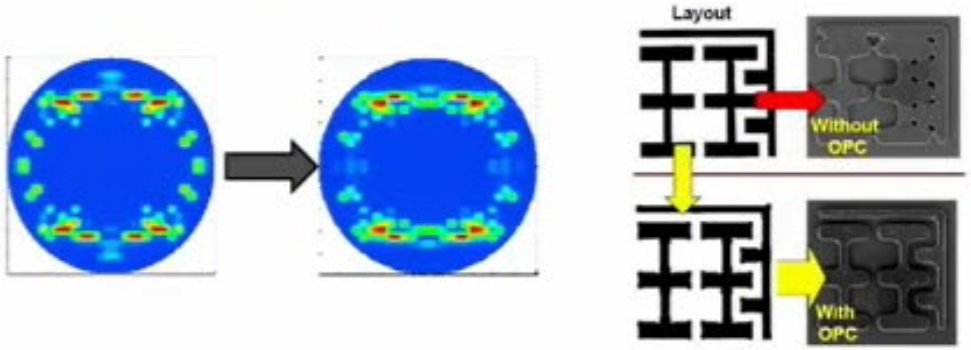
Single model and the same platform throughout is essential.

从设计到流片的流程



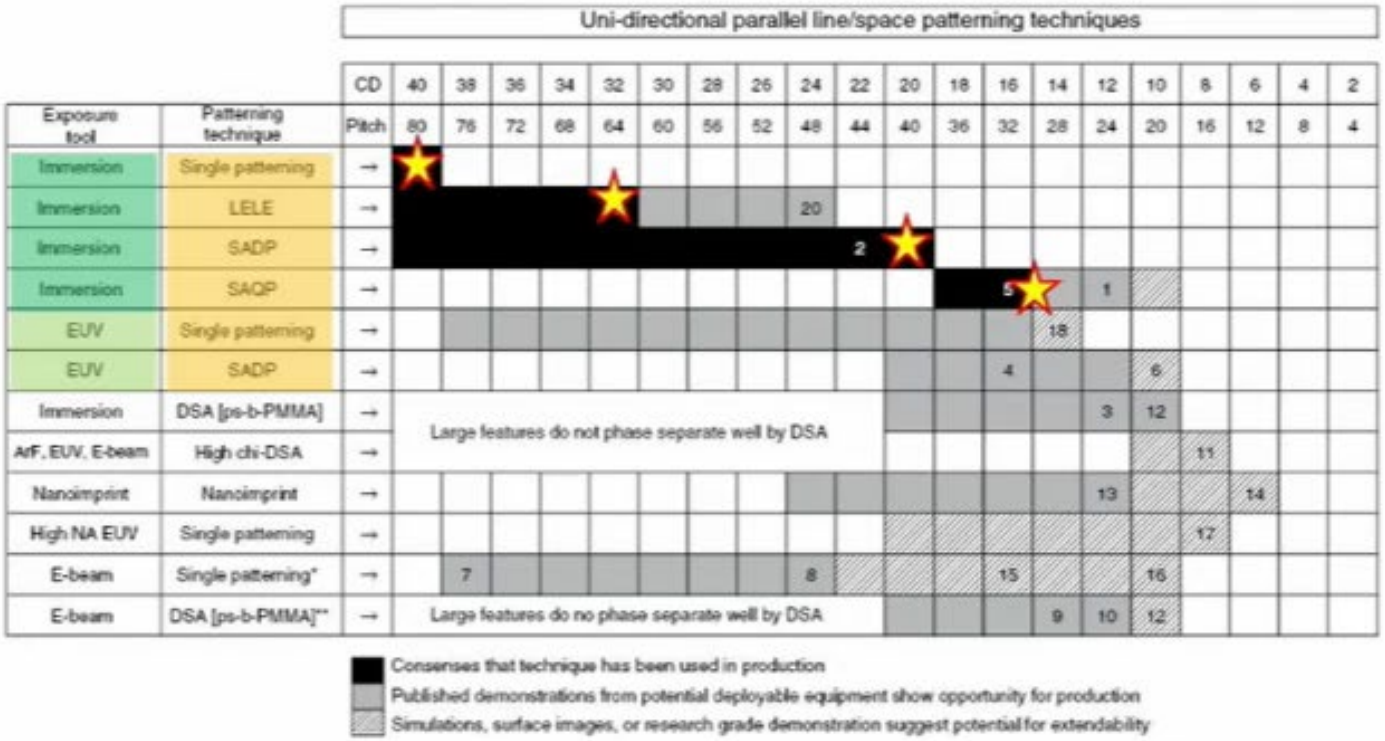
图形拆分技术

自对准多重成像技术



分辨率增强技术

多重成像技术（MPT）



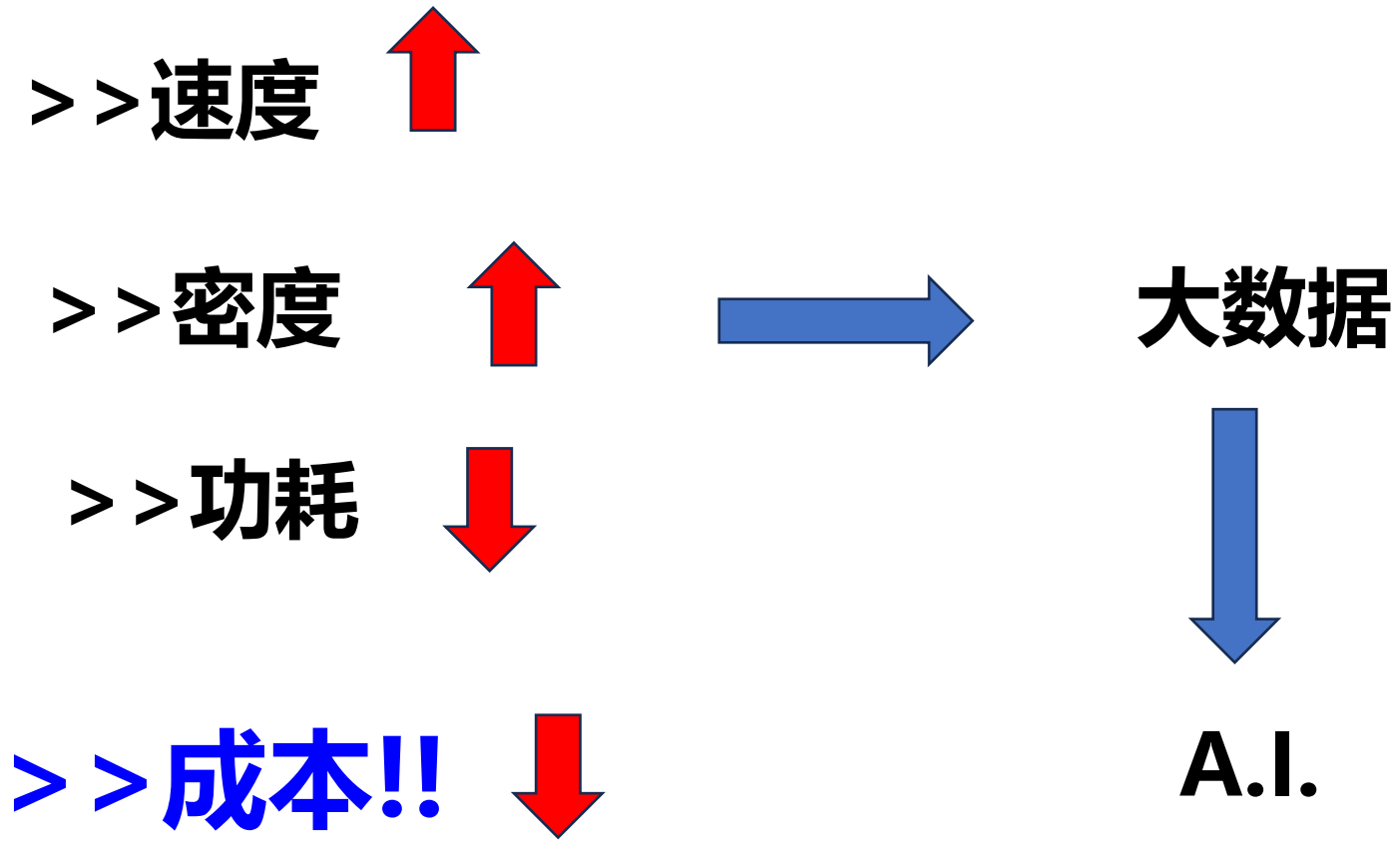
ITRS Lithography 2015

Pattern	Patterning Scheme	
	14nm	7nm
Fin	SADP	SAQP
Fin cut	2-cut	3-cut
Gate	Single	SADP
Gate cut	1 cut	1 cut
MOL Trench Silicide	Single + 1 cut	LEx3+ Tone Inversion
MOL Contact Hole	LEx2 + Design Constraint	LEx4 + Design Constraint
Metal	LEx2 Bi-direction	SADP Uni-direction Or LEx2 + cut
Metal cut		3 cut->2 cut
Via	Single	LEx3

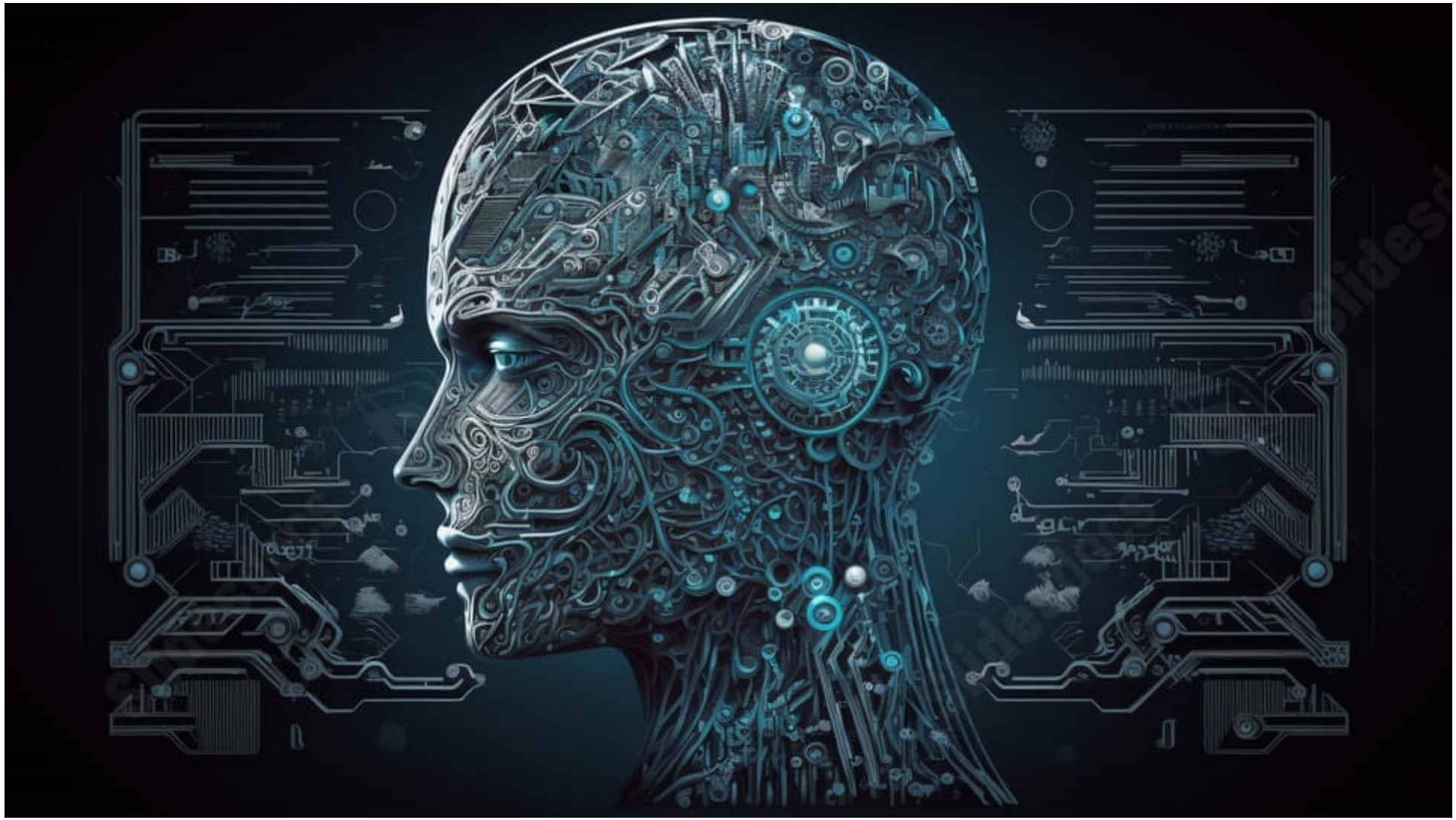
- **多重成像技术**是先进工艺技术节点实现更小图形周期和更高集成度的关键

摩尔定律

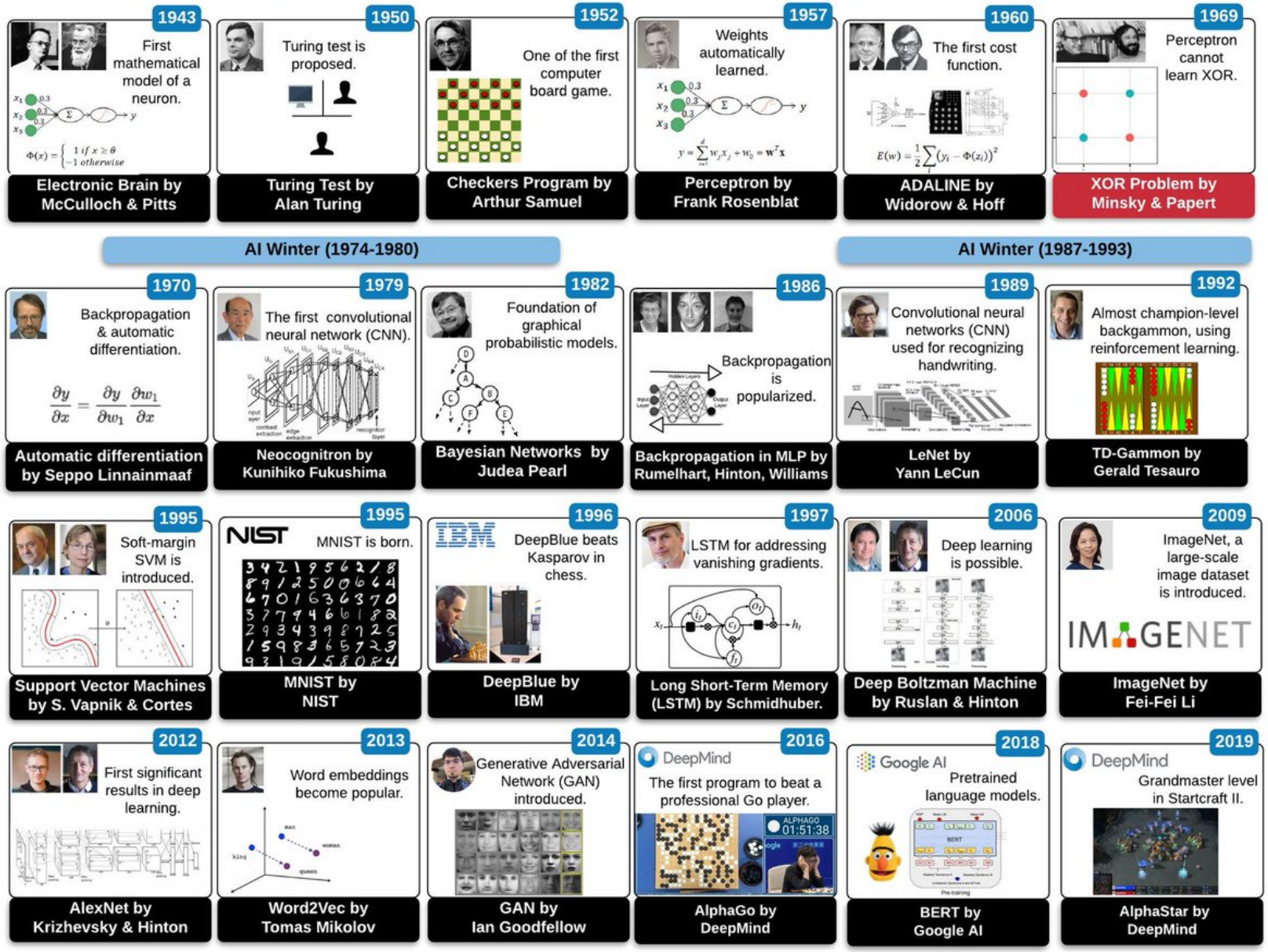
为什么要不断缩小器件尺寸?



人工智能



人工智能发展历史

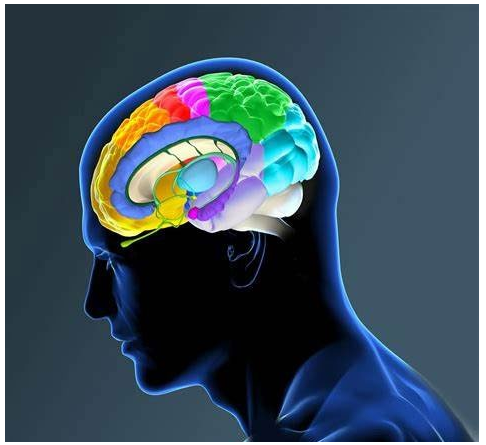


Parisa Rashidi, May 2020, CC BY 4.0

AlphaGo+Deeplearning

Hardware：
1920 CPU+200GPU
+lots of DRAM +lots of HDD
+lots of network

~MW Power



~20W Power

OpenAI, ChatGPT

ChatGPT

Examples

"Explain quantum computing in simple terms" →

"Got any creative ideas for a 10 year old's birthday?" →

"How do I make an HTTP request in Javascript?" →

Capabilities

Remembers what user said earlier in the conversation

Allows user to provide follow-up corrections

Trained to decline inappropriate requests

Limitations

May occasionally generate incorrect information

May occasionally produce harmful instructions or biased content

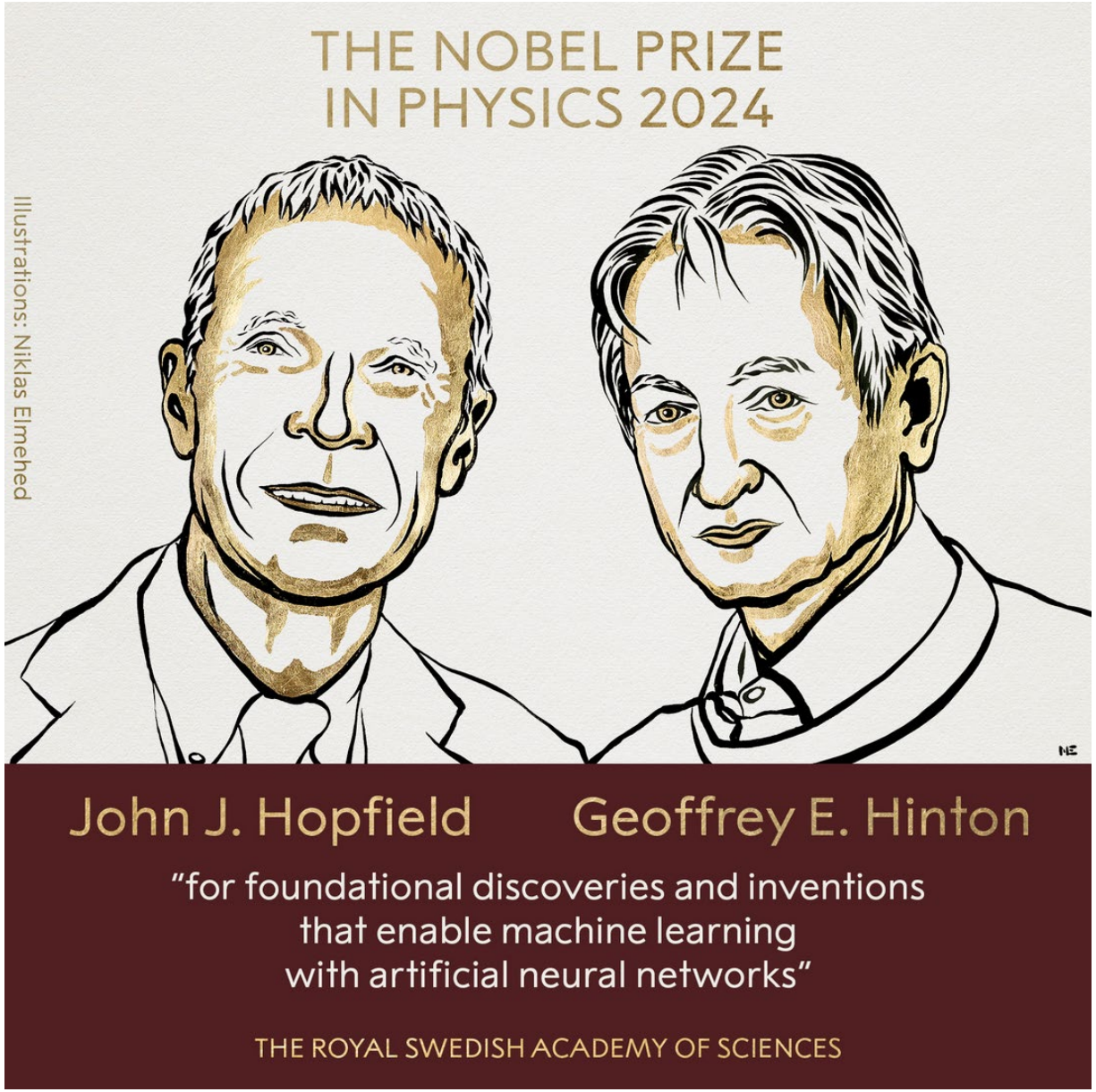
Limited knowledge of world and events after 2021

知乎 @泳鱼

《自然》2023年度十大科学人物榜单揭晓

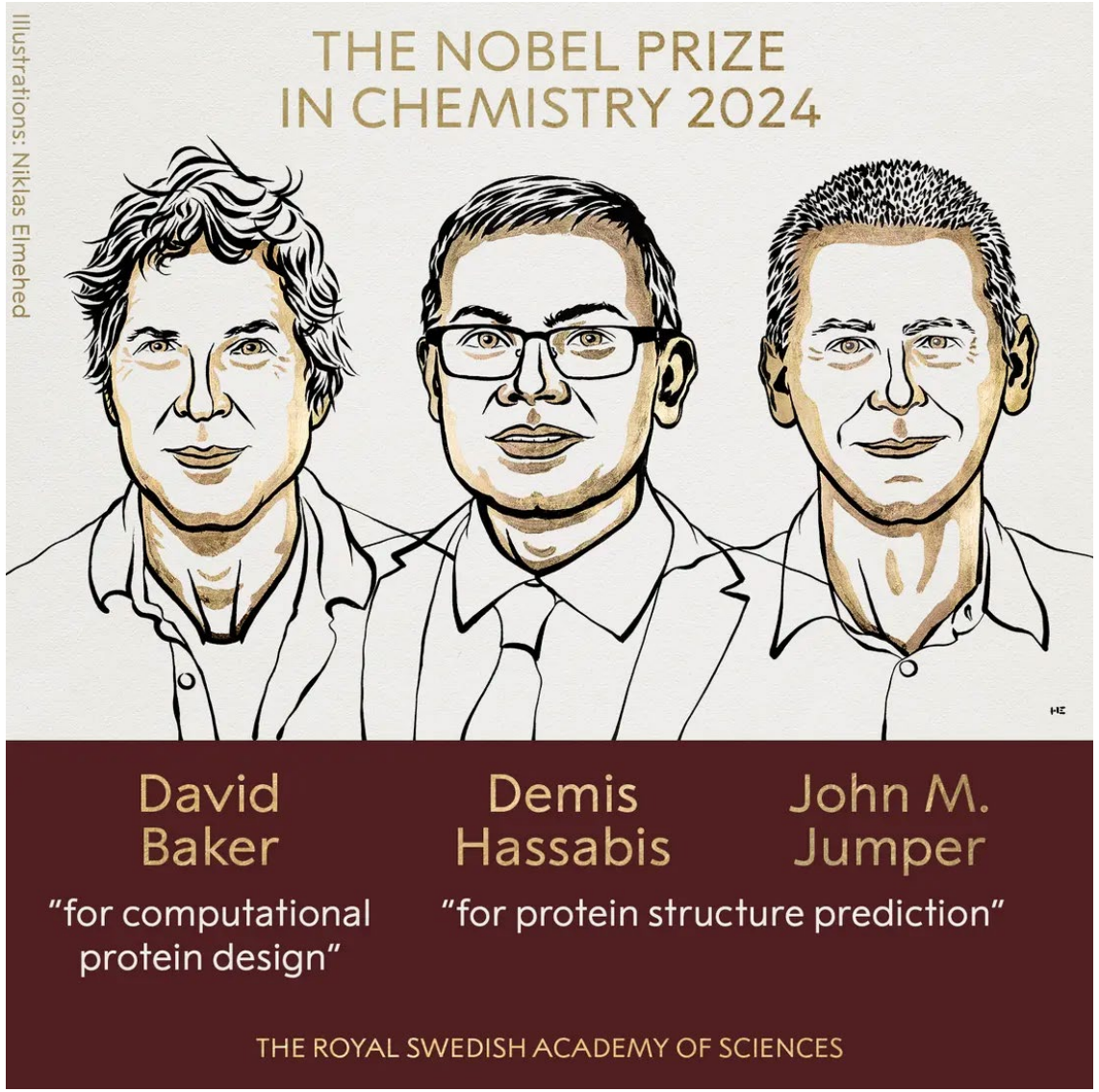
首次出现非人类

2024年诺贝尔物理学奖



2024年诺贝尔物理学奖授予了美国普林斯顿大学教授约翰·霍普菲尔德（John J. Hopfield）和加拿大多伦多大学教授杰弗里·辛顿（Geoffrey E. Hinton），以表彰他们“基于人工神经网络实现机器学习的基础性发现和发明”。他们使用物理学训练了人工神经网络，为当今强大的机器学习技术奠定了基础。

2024年诺贝尔化学奖



长期以来，化学家一直梦想着完全理解和掌握生命的化学工具——蛋白质。这个梦想现在已经触手可及。Demis Hassabis 和 John Jumper 成功地利用人工智能预测了几乎所有已知蛋白质的结构。David Baker 已经学会了如何掌握生命的组成部分并创造全新的蛋白质。他们的发现潜力是巨大的。

大卫·贝克

1962 年出生于美国华盛顿州西雅图。1989 年毕业于美国加州大学伯克利分校，获得博士学位。美国华盛顿州西雅图华盛顿大学教授和美国霍华德休斯医学研究所研究员。

“用于计算蛋白质设计”

DEMIS HASSABIS

1976 年出生于英国伦敦。2009 年在英国伦敦大学学院获得博士学位。Google DeepMind 首席执行官，英国伦敦。

JOHN JUMPER

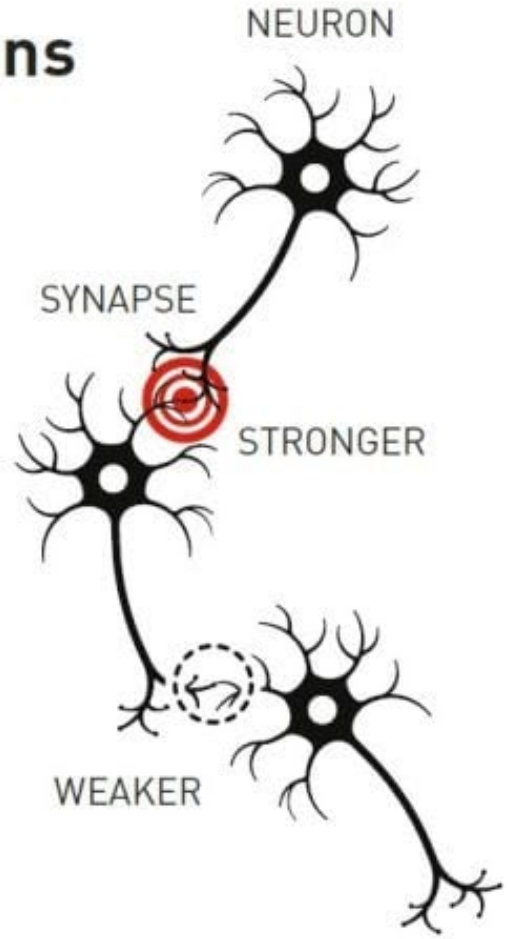
1985 年出生于美国阿肯色州小石城。2017 年获得美国伊利诺伊州芝加哥大学博士学位。英国伦敦 Google DeepMind 的高级研究科学家。

“用于蛋白质结构预测”

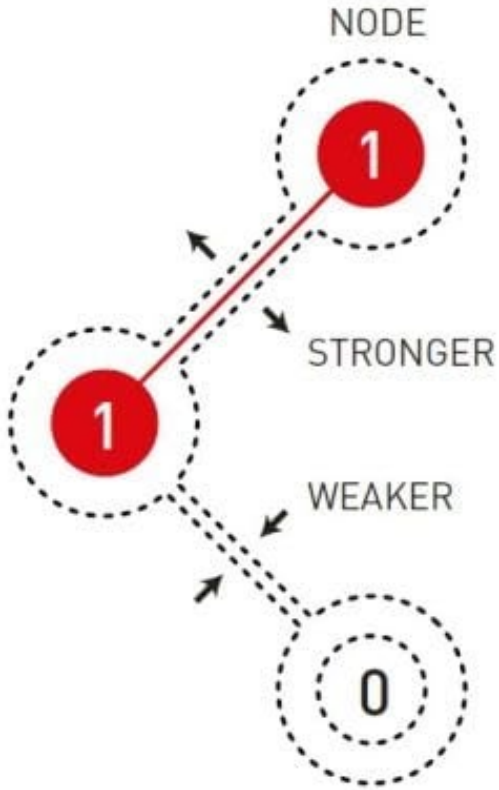
神经网络

Natural and artificial neurons

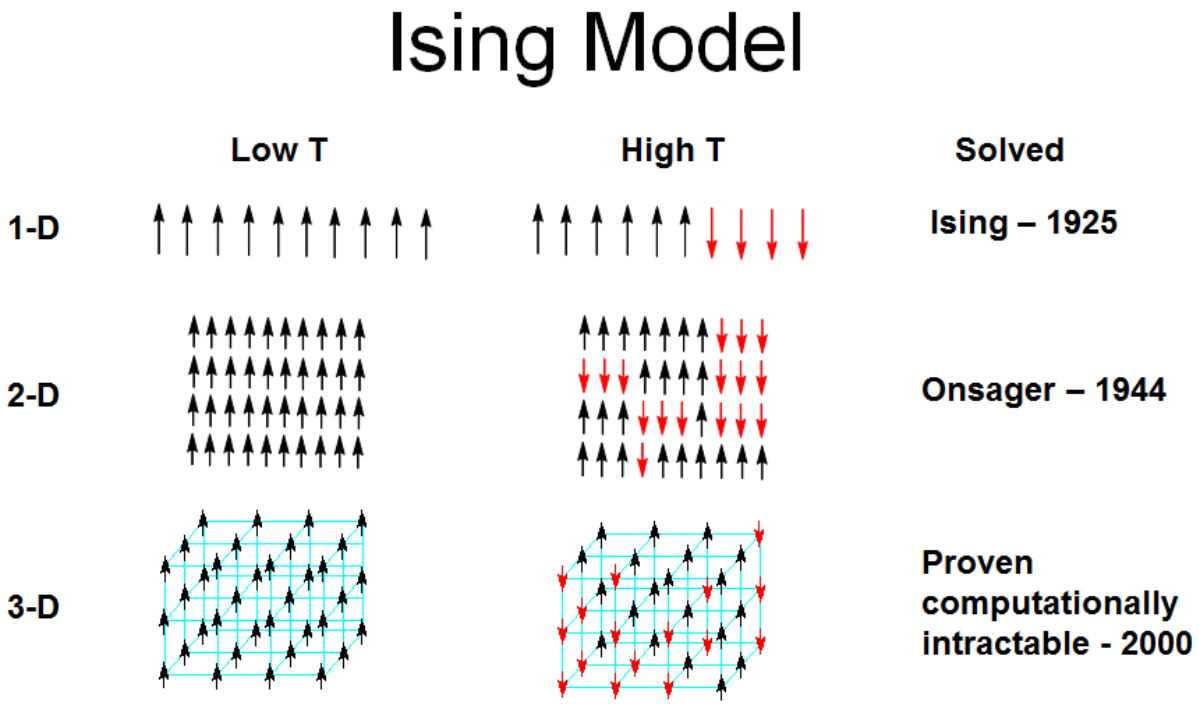
The brain's neural network is built from living cells, neurons, with advanced internal machinery. They can send signals to each other through the synapses. When we learn things, the connections between some neurons get stronger, while others get weaker.

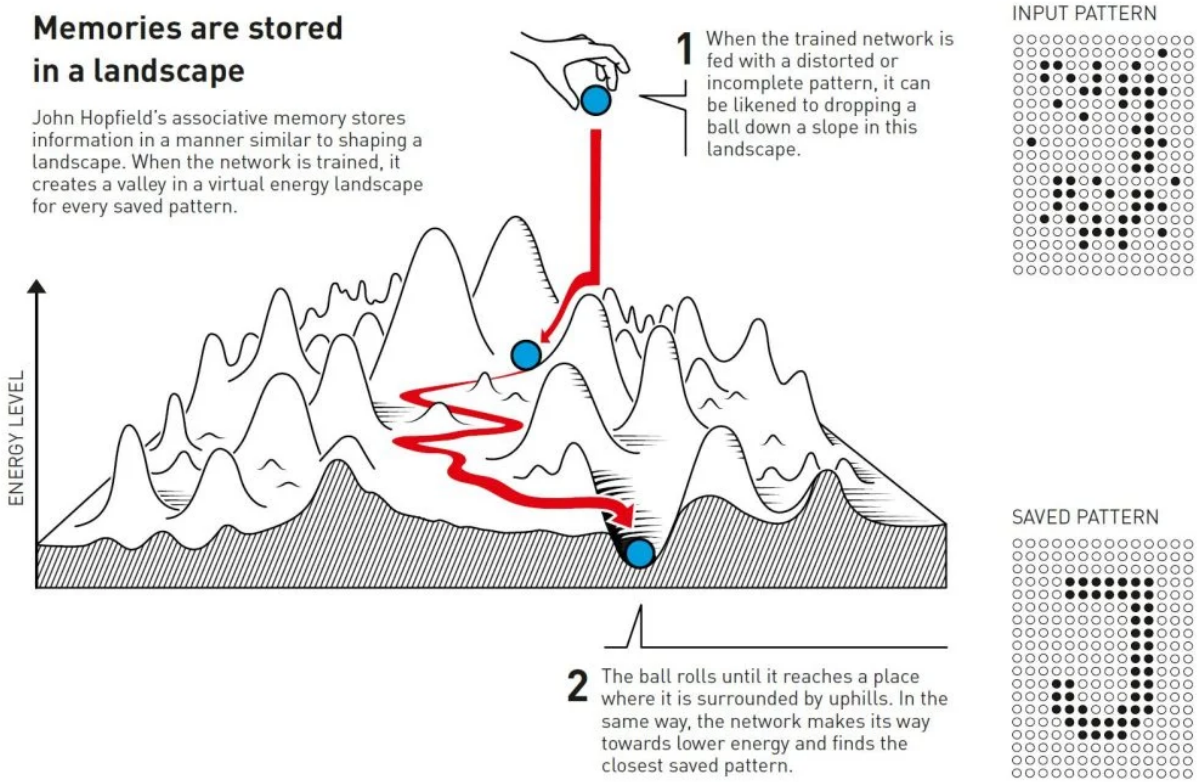


Artificial neural networks are built from nodes that are coded with a value. The nodes are connected to each other and, when the network is trained, the connections between nodes that are active at the same time get stronger, otherwise they get weaker.



Ising 模型和Hopfield神经网络





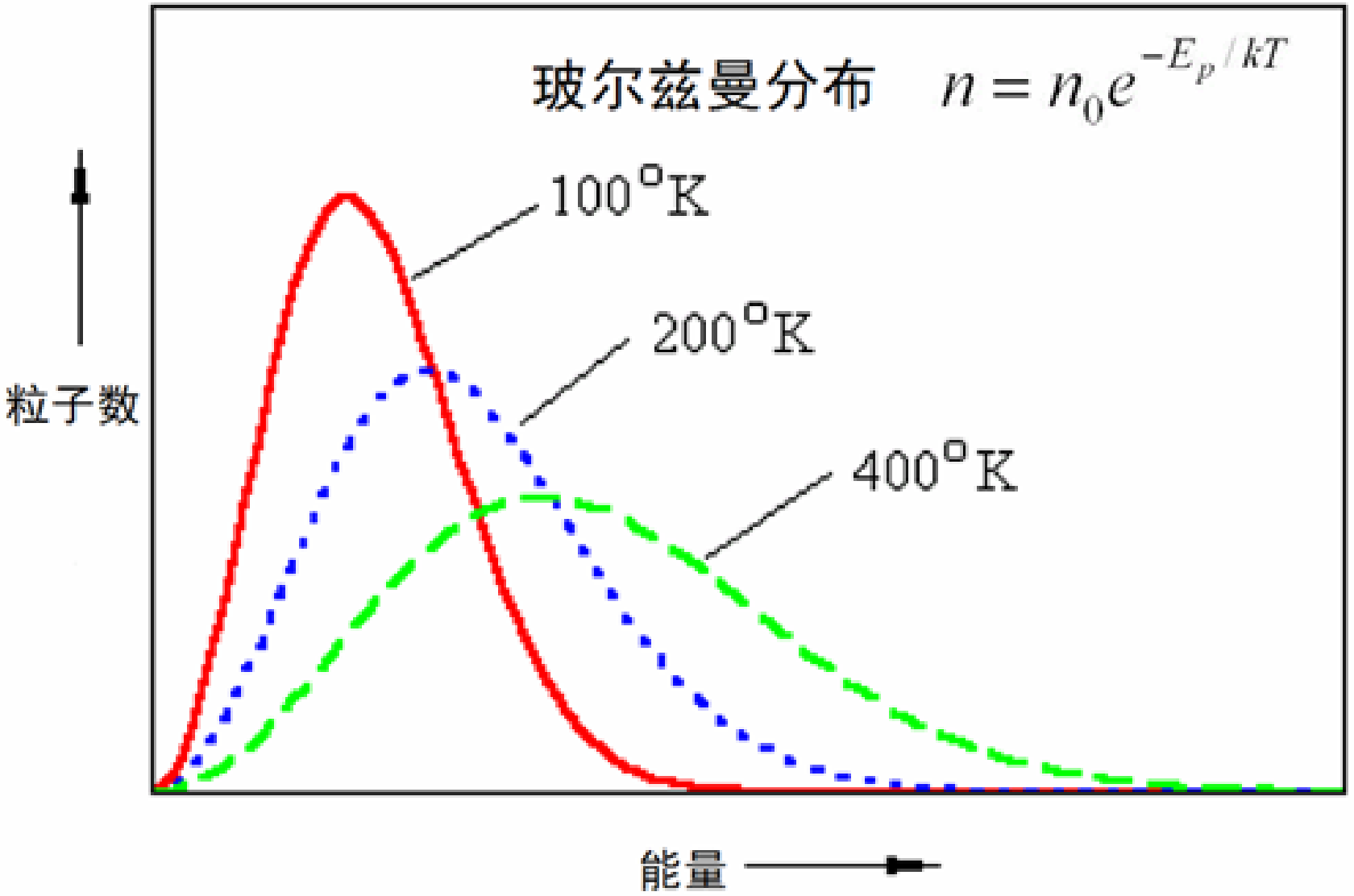
波尔兹曼机

1. 模拟退火

我们知道，
Hopfield神
度上升的方
为了解决这
题。'退火'是
体不处于最
形成高密度
Metropolis算
础。1953年
称为Metrop

局

如上图所示
力。而模拟



越高，混乱程度
力学平衡状态。
和玻尔兹曼分布
到一种基于概率的
点：初始温度可以
；在迭代的过程中，
即网络达到平衡
该足够慢，可以
。

温度为T

粒子总数为N

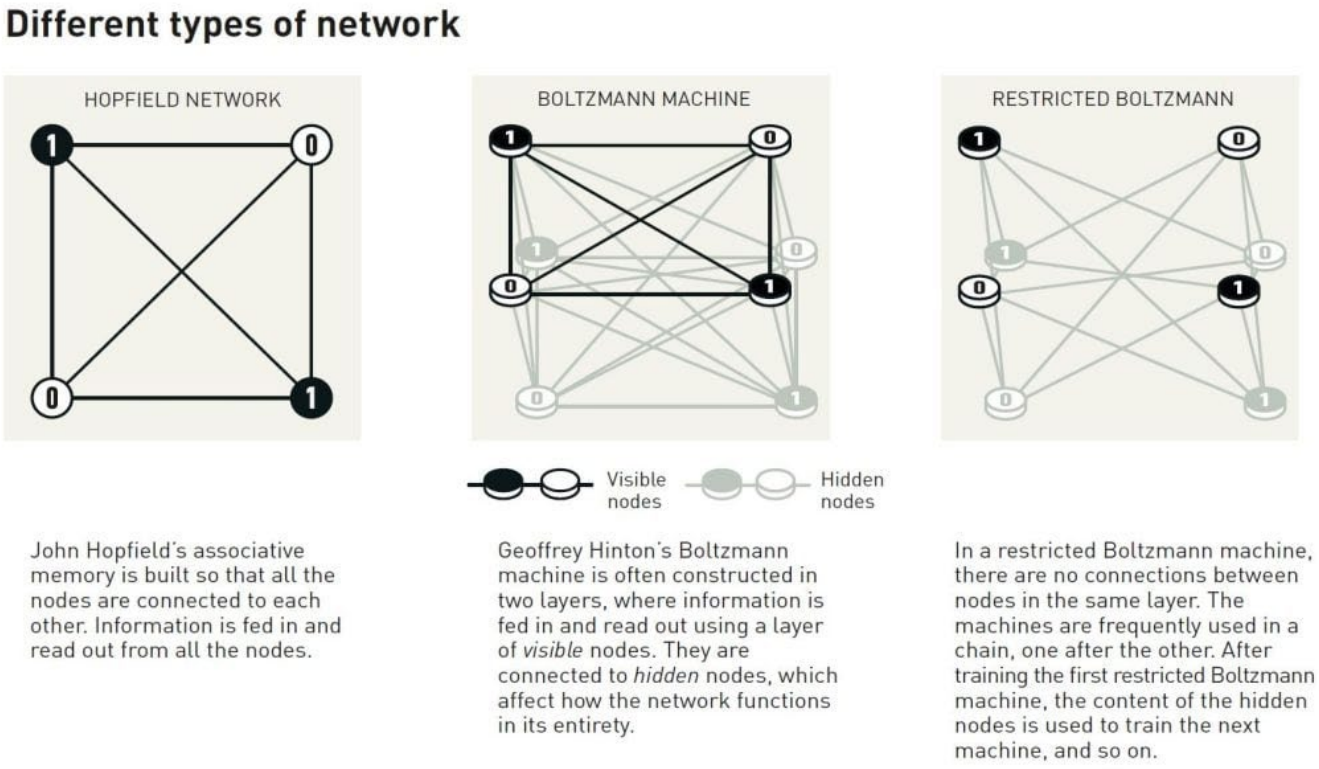
种粒子ε_0，ε_1

的能级上有n_0个
的能级上有n_1个
= N

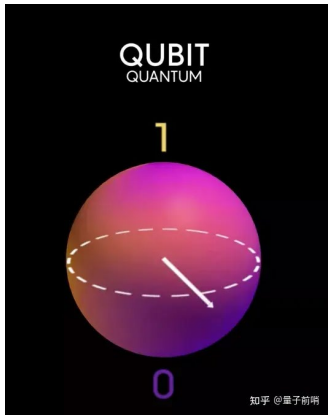
波尔兹曼机和深度学习

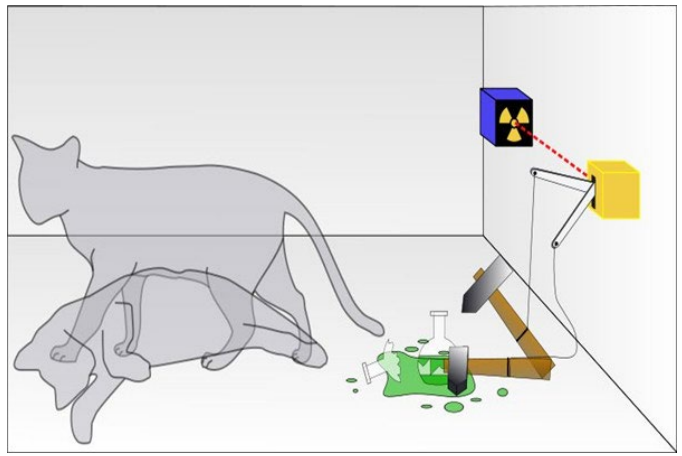
得益于 John Hopfield 和 Geoffrey Hinton 从 1980 年代开始的工作，他们帮助为 2010 年左右开始的机器学习革命奠定了基础。我们现在目睹的发展是通过访问可用于训练网络的大量数据以及计算能力的巨大提高而实现的。今天的人工神经网络通常非常庞大，由许多层构成。这些称为深度神经网络，它们的训练方式称为深度学习。

快速浏览一下 **Hopfield 1982 年关于联想记忆的文章，就可以为这一发展提供一些观点。在其中，他使用了一个具有 30 个节点的网络。如果所有节点都相互连接，则有 435 个连接。节点有其值，连接具有不同的强度，并且总共需要跟踪的参数不到 500 个。他还尝试了一个具有 100 个节点的网络，但考虑到他当时使用的计算机，这太复杂了。我们可以将其与今天的大型语言模型进行比较，这些模型被构建为可以包含超过 1 万亿个参数（100 万万个）的网络。**



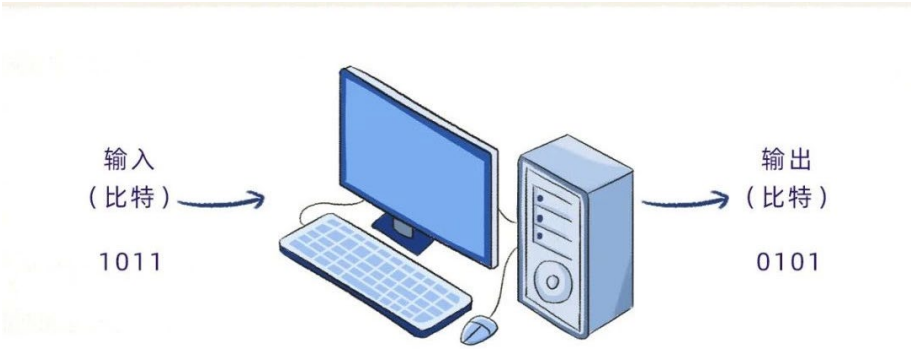
量子计算

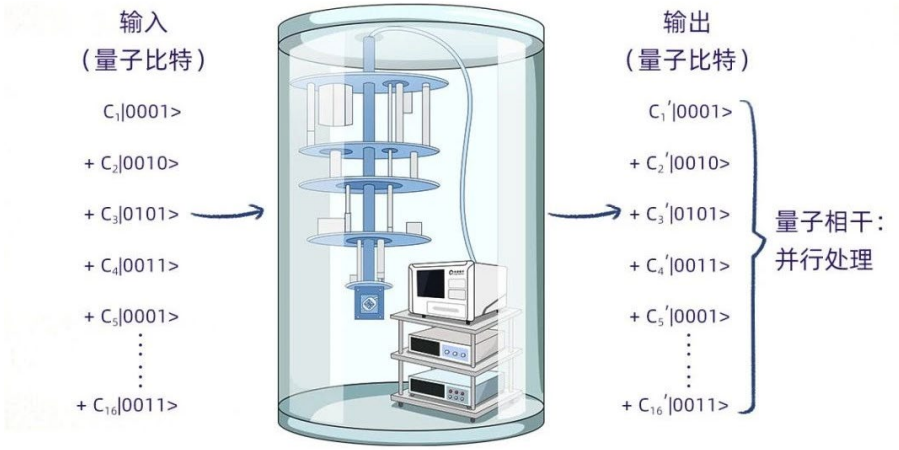




经典比特 0110101110110

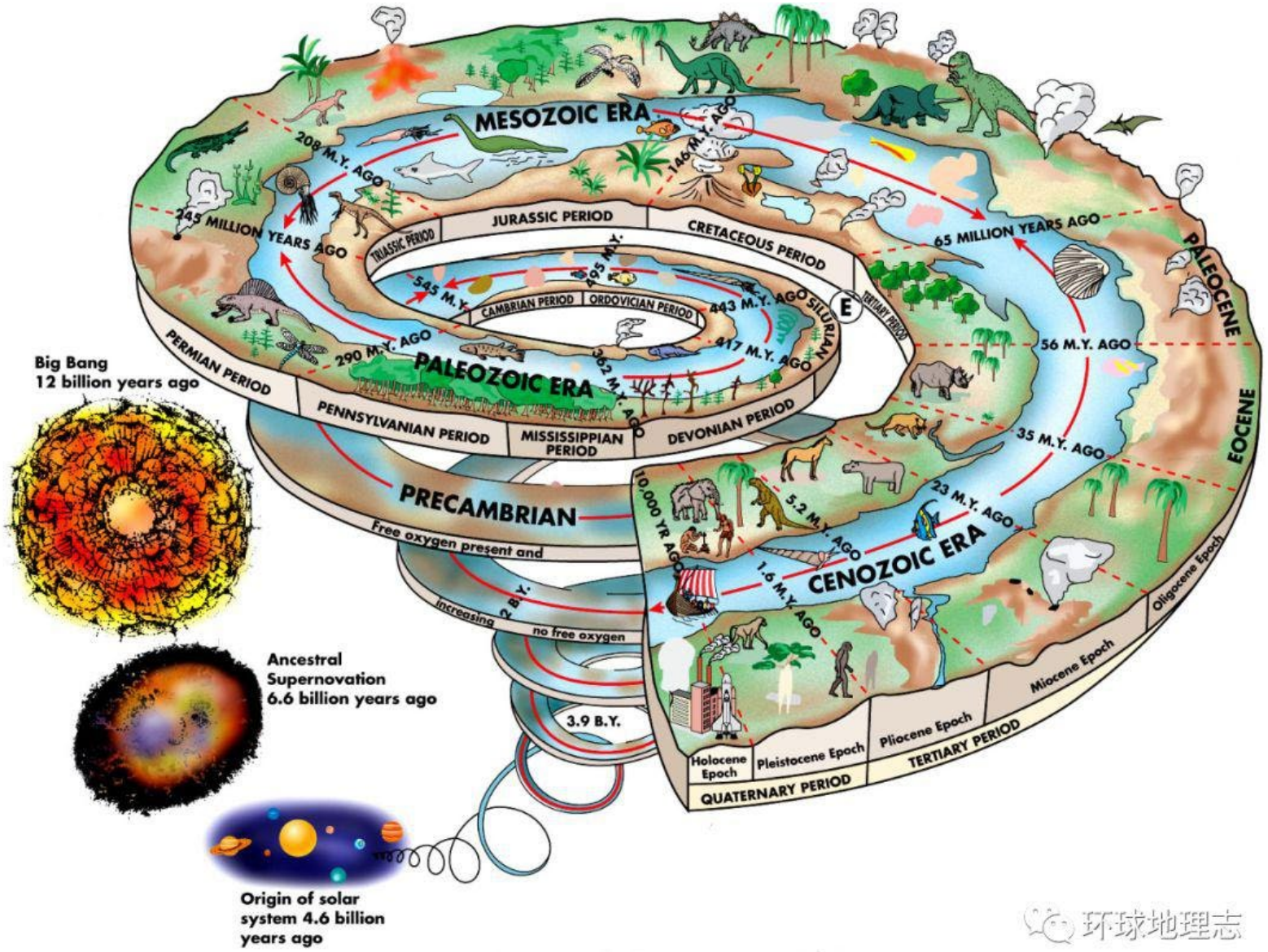
量子比特 0110101110110





脑机接口+A.I

宇宙和生命的起源



环球地理志

谢谢垂听
请指正